To: John Schafer (and Robert Nally)

I find these two patent applications strangely familiar.
Pay careful attention to Fig. 6 of "VARIABLE PIXEL DEPTH..." compared to the diagram on page 7 of R. Nally's Alpine video proposal!

The Alpine proposal is from 9-10-93
The patent application was filed 4-27-94
Note the name Vlad Bril as inventor
Note the lack of R. Nally.

Any questions?

Regards, Dave Keene

Pixel Semiconductor
A Cirrus Logic Company

CL-PX2070

Preliminary Data Sheet

Digital Video Processor

APPLICATIONS

- Presentation
- Video Editing
- Video Authoring
- Video Teleconferencing
- Interactive Education Systems
- Games

FEATURES

- Supports up to three simultaneous video data streams
- Video scaling
- Complete Frame Buffer control
- Interfaces to CODECs, decoders, encoders
- Integrated ISA, MCA, and host bus interface
- Supports both YCbCr and RGB formats
- 1/2 - 8 Mbytes of Frame Buffer memory

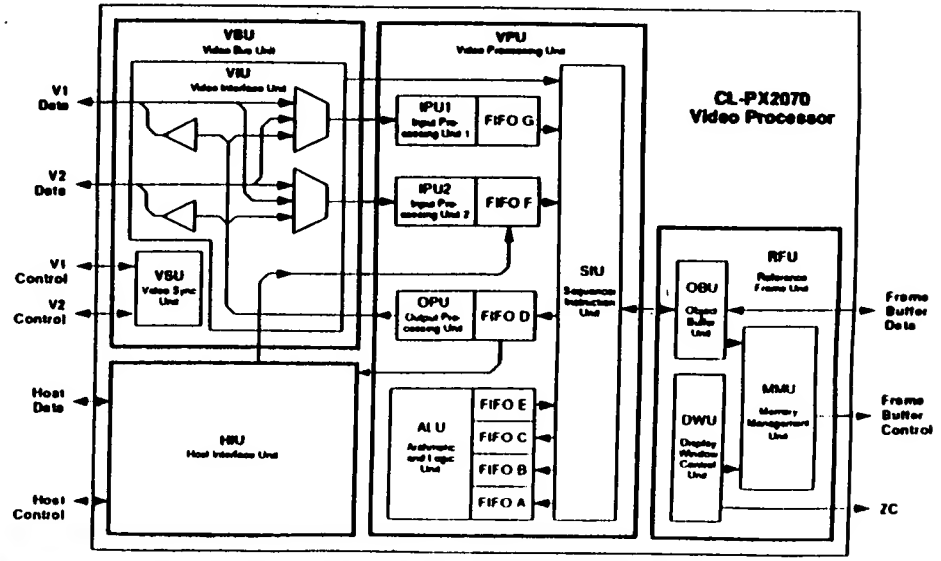
(cont. next page)

OVERVIEW

The CL-PX2070 Digital Video Processor provides a powerful, cost-effective solution on the desktop for computer graphics and imaging. The CL-PX2070 can be used in presentations, video teleconferencing, animation, and video capture for scaling with Video Signal Processors dedicated to compressing and decompressing video data streams.

(cont next page)

Functional Block Diagram



FEATURES (cont.)

- **Video stream format conversion**
- **Color space conversion**
- **Supports up to eight simultaneous object buffers**
- **Programmable, triple-channel LUT RAM**
- **Prescaling, zoom, and windowing**
- **Graphic and bit-mapped stream support**
- **Programmable sync slave or master**
- **When used with the CL-PX2070 MediaDAC™**
  - — Simultaneous video and graphics display
  - — Four simultaneous, overlapping (occluded) display windows
  - — Zooms from 1x to 256x
  - — 1024 x 768 display at 85 MHz

OVERVIEW (cont.)

The CL-PX2070 extends the real time video scaling features of the CL-PX0070 VWG by combining the Frame Buffer memory management, arithmetic and logical processing, a programmable host system bus interface, flexible mainstream video datapath, and windowing control for multiple simultaneous video data streams.

The CL PX2070 has four major functional units.

- HIU: Host Interface Unit
- VBU: Video Bus Unit
- VPU: Video Processing Unit
- RFU: Reference Frame Unit

HIU: Host Interface Unit

The HIU interfaces the CL PX2070 to the host system. The unit supports high speed DMA transfers of graphic or video data between the host system and the Frame Buffer through direct access to FIFOs in the Video Processing Unit, and provides access to the CL-PX2070 control registers.

VBU: Video Bus Unit

The VBU manages the flow of video and graphic streams between the CL-PX2070 and up to three independent devices (including the host system). It also provides a data path between the CL-PX2070 and the host system for bidirectional graphic streams through the HIU.

The VBU provides two independent, real-time video I/O ports, and contains two subunits — VIU and VSU.

Video ports V1 and V2 have the following characteristics:

- Each can be configured as input only, output only, or pixel- or field duplexed I/O;
- Each provides programmable sync polarity;
- Either port can use the sync generator provided by the CL-PX2070;
- Each supports the following formats:
  - -- 16 bit 4:2:2 YCbCr, 12-bit 4:1:1 YCbCr, 16-bit RGB, 8 bit RGB (input),
  - — 16 bit YCbCr, 16-bit RGB, 8-bit RGB (output);

	ISA Bus Interface	MCA Bus Interface	Local Hardware Interface
Interface	CL PX2070 interfaces with the host system interface bus		CL-PX2070 interfaces with the processor bus
Multiplex Support	CL PX2070 signals support the required host system address/data multiplexing, and provide bidirectional buffering of the host system data bus		N/A
Address Decode	CL PX2070 internally decodes the bus address during system I/O cycles		The host system provides the decoded chip select signal for use with register select input signals
DMA	DMA through I/O port	N/A	DMA through indexed port or I/O port

- V2 controls the video stream data flow between the CL-PX2070 and typical CODEC devices.

The VIU (Video Interface Unit) controls the flow of internal video streams through the video ports to all external devices. It specifies:

- the source and direction of video stream and sync control inputs;
- the Field-toggling Mode and field ID signals;
- the watchdog timer feature.

The VSU (Video Sync Unit) implements identical, independent reference signals for each video port:

- Vertical sync specifies the beginning of a field or frame.
- Horizontal sync specifies the beginning of a line.
- Horizontal/composite blanking specifies the horizontal/ composite blanking interval.

Each video port independently controls sync polarity for each of these signals. Two VIU master control registers provide matching fields that specify input and output sync modes. FIFO-D can send to, and FIFO-F can receive from, the HIU directly.

VPU: Video Processing Unit

The VPU provides field-oriented video processing. It can simultaneously process two external, bidirectional real-time video streams and a single external, bidirectional host video or graphic data stream.

As shown in the functional block diagram on the cover, the VPU has five subunits: the IPU1, IPU2, OPU, ALU, and SIU.

The IPU1 (Input Processor Unit 1) prepares an input video stream for ALU processing and/or storage in the Frame Buffer, then outputs the prepared stream to the Frame Buffer Data Bus. Its video processing features include:

- YCbCr and RGB input stream format conversion,
- color space conversion,
- programmable data tagging,
- three-channel lookup table operations,
- horizontal prescaling,
- window clipping,
- horizontal and vertical scaling, and
- output stream format conversion.

The IPU2 (Input Processor Unit 2) provides prescaling and windowing.

The OPU (Output Processing Unit) provides zoom, window clipping, and output-format functions.

The ALU (Arithmetic Logic Unit), shown below, performs logical and tagging operations for RGB and 8 bit pseudo color streams. The ALU also performs arithmetic, logical, and tagging operations for YCbCr streams. Its registers control stream format, operand source selection, tagging operation selection, and arithmetic or logical operation for both field times. The ALU can process up to three simultaneous video streams input through its FIFOs.

The SIU (Sequencer Instruction Unit) is a special-purpose microcontroller that coordinates the flow of multiple, simultaneous data streams between the IPU1, IPU2, OPU, ALU, and OBU.

The SIU is field based when processing interlaced-video data, distinguishing between the vertical sync pulses for each field and executing one of two different instruction sequences. The manner in which it executes these instructions causes multiple stream flows to appear concurrent.

RFU: Reference Frame Unit

The RFU provides simultaneous access to eight object buffers and four display windows. It has three subunits — OBU, DWU, and MMU.

The OBU (Object Buffer Unit) allows each object buffer to be locked to either video source, or to be programmed to operate independently. Object buffers may also be placed anywhere within the linearly-addressable Frame Buffer. OBU Registers specify the size, location, operating mode, X and Y raster directions, FIFO association, chrominance and luminance channel masking, and output destination for each object buffer.

The DWU (Display Window Unit) allows each display window to be any size or location. When used with the CL PX2080, display windows can overlap.

The MMU (Memory Management Unit) provides the Frame Buffer control interface for up to 8 Mbytes of DRAM or VRAM.

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CONVENTIONS, ABBREVIATIONS, AND TRADEMARKS

CONVENTIONS

Conventions used in this document are described in the following example:

VIU_DPCf	Register names that contain lower-case variables represent groups of registers with similar functions. For example, VIU_DPCf represents both of the Datapath Control registers — register VIU_DPC1 (Datapath Control Field 1) and register VIU_DPC2 (Datapath Control Field 2). Table 4-1 on page 84 defines all variables used in this manner.

ABBREVIATIONS, ACRONYMS, and MNEMONICS

Abbreviations, acronyms, and mnemonics used in this document are described in the following table:

ALU	Arithmetic and Logic Unit
CODEC	Code/Decode or Compress/decompress
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CTAG	Control Tag Multiplexer signal
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DWU	Display Window Unit
FBU	Frame Buffer Data
FIFO	First In First Out
ISA	Industry Standard Architecture
I/O	Input / Output
LSA	Linear Start Address
JPEG	Joint Photographic Expert Group
LSB	Least Significant Byte
LSb	Least Significant bit
LUT	Look Up Table
MCA	Micro Channel Architecture
MMU	Memory Management Unit
MSB	Most Significant Byte

MSb	Most Significant bit
OPU	Output Processor Unit
OTAG	Output Tag Multiplexer signal
IPU1	Input Processor Unit 1
IPU2	Input Processor Unit 2
POFP	Plastic Quad Flat Pack
PSE	PreScaler Enable
RGB	Red, Green, Blue
RAM	Random Access Memory
RFU	Reference Frame Unit
SIM	Sequencer Instruction Memory
SIU	Sequencer Instruction Unit
VPU	Video Processor Unit
VRAM	Video Dynamic Random Access Memory
YCbCr	Components of the CCIR601 color representation standard. Luminance, Y blue, Y red (color difference values)

TRADEMARKS

Trademarks used in this document are described in the following table:

MediaDAC™ is a trademark of Pixel Semiconductor, Inc.

1. PIN INFORMATION

The CL-PX2070 is available in a 160 lead Plastic Quad Flat Pack (PQFP) surface-mount package. It can be configured for ISA, MCA, and local hardware interface configurations, as shown in Figure 1-1, Figure 1-2, and Figure 1-3.

NOTE: (*) denotes active low signals

1.1 Pin Diagrams

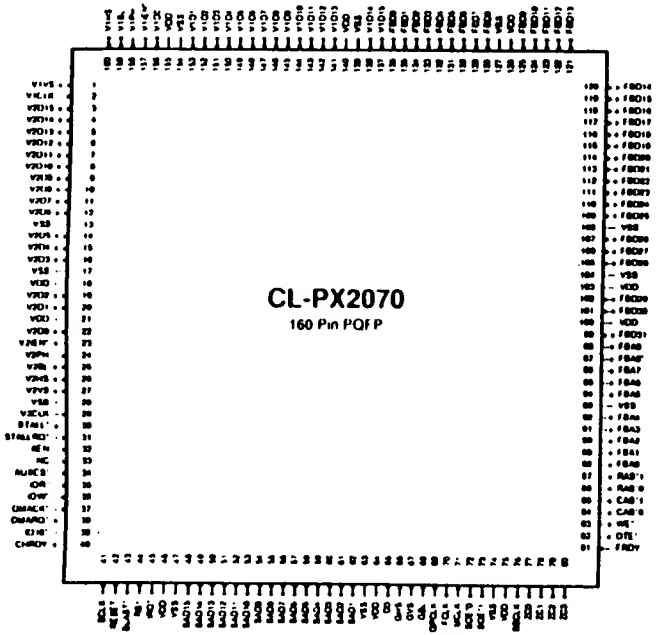


Figure 1-1. Pin Diagram — ISA Bus Interface

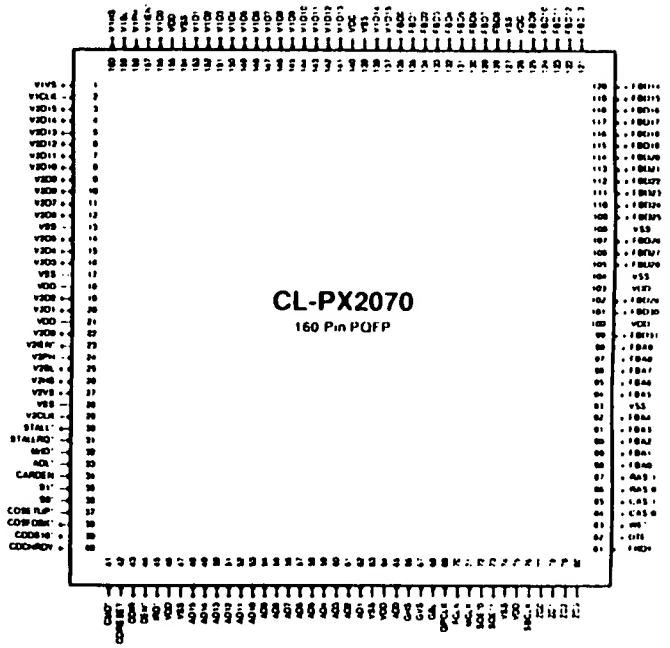


Figure 1-2. Pin Diagram — MCA Bus Interface

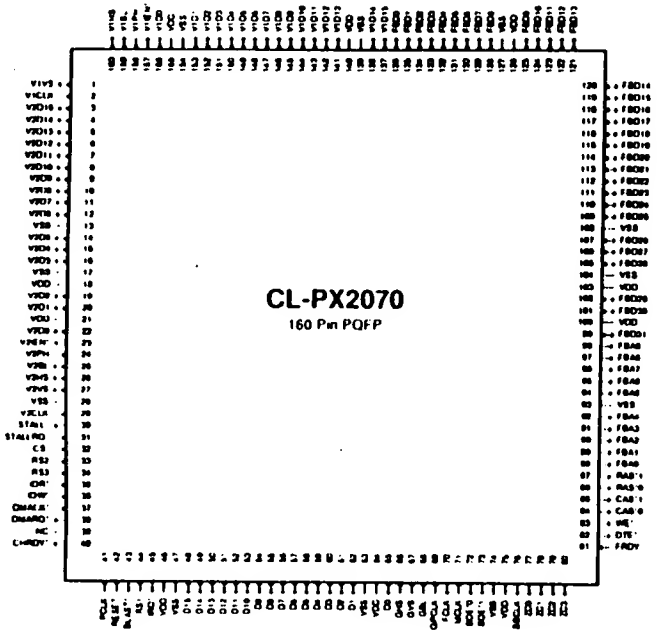


Figure 1-3. Pin Diagram — Local Hardware Interface

1.2 Pin Assignment Table

The following conventions are used in the pin assignment table

- * = active low signal
- I = input
- O = output
- I/O = input/output
- PWR = power
- TTL = the pad has standard TTL input threshold and output levels
- OD = open drain, TTL inputs
- 4 = 4 mA sink and 2 mA source drive capability
- 24 = 24 mA sink and 8 mA source drive capability
- N/A = not applicable

NAME	PIN	TYPE	CELL	FUNCTION
PROCESSOR INTERFACE — ISA BUS MODE				
SAD[15:0]	48,62, 65	I/O	TTL, 4	Address/Data Bus
DEN*	44	OD	TTL, 8	Data Buffer Enable
DDIR	43	OD	TTL, 8	Data Buffer Direction
IOR*	35	I	TTL	I/O Read
IOW*	36	I	TTL	I/O Write
AEN	32	I	TTL	Address Enable
DMARQ	38	O	TTL, 4	DMA Request
DMACK*	37	I	TTL	DMA Acknowledge
IRQ	45	O	TTL, 4	Interrupt Request
CHRDY	40	OD	TTL, 24	Channel Ready
IO16*	39	OD	TTL, 24	16 bit I/O Cycle
BCLK	41	I	TTL	Bus Clock
RESET	42	I	TTL	Reset
NC	33	N/A	N/A	No Connect (must be left floating)
AUXCS*	34		TTL	Auxiliary Chip Select
PROCESSOR INTERFACE — MCA BUS MODE				
AD[15:0]	48,62, 65	I/O	TTL, 4	Address/Data Bus
DEN*	44	OD	TTL, 8	Data Buffer Enable
DDIR	43	OD	TTL, 8	Data Buffer Direction
S1*	35	I	TTL	Status 1
S0*	36	I	TTL	Status 0
CARDEN	34	I	TTL	Card Enable
M/IO*	32	I	TTL	Memory or I/O Cycle
CDSFDBK*	38	O	TTL, 4	Card Select Feedback
CDSETUP*	37	I	TTL	Card Setup
IRQ*	45	O	TTL, 4	Interrupt Request
CDCHRDY	40	OD	TTL, 24	Channel Ready
CDDS16*	39	OD	TTL, 24	Card Data Size
CMD*	41	I	TTL	Command
CDRESET	42	I	TTL	Reset
ADL*	33	I	TTL	Address Latch

NAME	PIN	TYPE	CELL	FUNCTION (cont.)
PROCESSOR INTERFACE — LOCAL HARDWARE INTERFACE MODE				
D[15:0]	48 62, 65	I/O	TTL, 4	Data Bus
RS[3:1]	34 33, 44	I	TTL	Register Select
BLAST*	43	O	TTL, 4	Burst Last
IOR*	35	I	TTL	I/O Read Cycle
IOW*	36	I	TTL	I/O Write Cycle
CS*	32	I	TTL	Chip Select
DMARQ*	38	O	TTL, 4	DMA Request
DMACK*	37	I	TTL	DMA Acknowledge
IRQ*	45	O	TTL, 4	Interrupt Request
CHRDY*	40	OD	TTL, 24	Channel Ready
PCLK	41	I	TTL	Processor Clock
RESET	42	I	TTL	Reset
NC	39	N/A	N/A	No Connect (must be left floating)
GRAPHICS OVERLAY INTERFACE				
GPCLK	69	I	TTL	Pixel Clock
GVS	67	I	TTL	Vertical Sync
GHS	66	I	TTL	Horizontal Sync
GBL	68	I	TTL	Blanking
VIDEO PORT 1 INTERFACE				
V1CLK	2	I	TTL	Video Data Clock
V1D[15:0]	137 138, 141 153, 156	I/O	TTL, 4	Video Data Bus
V1VS	1	I/O	TTL, 4	Vertical Sync
V1HS	160	I/O	TTL, 4	Horizontal Sync
V1BL	159	I/O	TTL, 4	Horizontal/Composite Blanking
V1PH	158	I	TTL	Phase
V1IEN*	157	O	TTL, 4	Input Enable
VIDEO PORT 2 INTERFACE				
V2CLK	29	I	TTL	Video Data Clock
V2D[15:0]	3 12, 14 16, 19 20, 22	I/O	TTL, 4	Video Data Bus
V2VS	27	I/O	TTL, 4	Vertical Sync
V2HS	26	I/O	TTL, 4	Horizontal Sync
V2BL	25	I/O	TTL, 4	Horizontal/Composite Blanking
V2PH	24	I	TTL	Phase
V2IEN*	23	O	TTL, 4	Input Enable
STALLRQ*	31	I	TTL	Stall Request
STALL*	30	O	TTL, 4	Stall

NAME	PIN	TYPE	CELL	FUNCTION (cont.)
FRAME BUFFER INTERFACE				
FBD[31:0]	99, 101 102, 105 107, 109 125, 128 136	I/O	TTL, 4	Data Bus
FBA[9:0]	98 94, 92 88	O	TTL, 8	Address Bus
RAS[1:0]*	87 86	O	TTL, 8	Row Address Strobes
CAS[1:0]*	85 84	O	TTL, 8	Column Address Strobes
WE*	83	O	TTL, 12	Write Enable
DTE*	82	O	TTL, 12	Data Transfer Enable
FRDY	81	I	TTL	FIFO Ready
ZC[3:0]	80 77	O	TTL, 4	Zoom Control Bus
SBCLK	76	O	TTL, 8	Serial Bus Clock
SOE[1:0]*	73 72	O	TTL, 8	VRAM Serial Port Output Enable
MCLK	71	I	TTL	Memory Clock
FCLK	70	O	TTL, 8	FIFO Write Clock
POWER				
VDD	18, 21, 46, 64, 75, 100, 103, 126, 140, 155	PWR	N/A	+5 VDC for Digital Logic and Interface Buffers
VSS	13, 17, 28, 47, 63, 74, 93, 104, 108, 127, 139, 154	PWR	N/A	Ground for Digital Logic and Interface Buffers

2. DETAILED SIGNAL DESCRIPTIONS

2.1 Processor Interface — ISA Bus Mode

Signal	Pin	Type	Cell	Function
SAD[15:0]	48,62, 65	I/O	TTL, 4	**Address/Data Bus:** Bidirectional, multiplexed address/data bus that transfers video data between the host system and the CL-PX2070
DEN*	44	OD	TTL, 8	**Data Buffer Enable:** When pulled low, enables the host data bus buffer
DDIR	43	OD	TTL, 8	**Data Buffer Direction:** Specifies the direction of data flow. When high, the host system is writing data to SAD[15:0]; when low, the host system is reading data from SAD[15:0]
IOR*	35	I	TTL	**I/O Read:** Specifies an I/O read cycle
IOW*	36	I	TTL	**I/O Write:** Specifies an I/O write cycle
AEN	32	I	TTL	**Address Enable:** Specifies that a DMA cycle is in progress
DMARQ	38	O	TTL, 4	**DMA Request:** Specifies that the CL-PX2070 is requesting a DMA transfer
DMACK*	37	I	TTL	**DMA Acknowledge:** Specifies that the host system is ready to perform a DMA transfer.
IRQ	45	O	TTL, 4	**Interrupt Request:** Specifies that the CL-PX2070 is requesting service from the host system
CHRDY	40	OD	TTL, 24	**Channel Ready:** When pulled low, specifies that the CL-PX2070 is not ready to complete the current host access cycle. The CL-PX2070 releases CHRDY to indicate that the current host access cycle should be completed
IO16*	39	OD	TTL, 24	**16-bit I/O Cycle:** Specifies that the CL-PX2070 is able to respond as a 16 bit I/O data device for both read and write cycles
BCLK	41	I	TTL	**Bus Clock:** Clock input used to synchronize access between the host system and the CL-PX2070
RESET	42	I	TTL	**Reset:** Causes the CL-PX2070 to cease all activity and perform a hardware reset
NC	33	N/A	N/A	**No Connect:** (must be left floating)
AUXCS*	34		TTL	**Auxiliary Chip Select:** When programmed for AuxISA Mode, primary and secondary addresses are ignored. AUXCS* and SAD[3:1] select specific registers

2.2 Processor Interface — MCA Bus Mode

Signal	Pin	Type	Cell	Function
AD[15:0]	48,62, 65	I/O	TTL, 4	**Address/Data Bus:** Bidirectional, multiplexed address/data bus that transfers video data between the host system and the CL-PX2070
DEN*	44	OD	TTL, 8	**Data Buffer Enable:** When pulled low, enables the host data bus buffer
DDIR	43	OD	TTL, 8	**Data Buffer Direction:** Specifies the direction of data flow. When high, the host system is writing data to SAD[15:0]; when low the host system is reading data from SAD[15:0]
S1*	35	I	TTL	**Status 1:** Used with M/IO* and S0* to specify the current bus cycle (see table under M/IO*)
S0*	36	I	TTL	**Status 0:** Used with M/IO* and S1* to specify the current bus cycle (see table under M/IO*)
CARDEN	34	I	TTL	**Card Enable:** Specifies that the data on bus AD[15:8] is valid
M/IO*	32	I	TTL	**Memory or I/O Cycle:** Used with S1* and S0* to specify the current bus cycle M/IO* S0* S1* 0 0 0 Reserved 0 0 1 I/O Write 0 1 0 I/O Read 0 1 1 Inactive 1 0 0 Reserved 1 0 1 Memory Write 1 1 0 Memory Read 1 1 1 Inactive
CDSFDBK*	38	O	TTL, 4	**Card Select Feedback:** Specifies that the CL-PX2070 has decoded the current address and status inputs. The CL-PX2070 does not drive CDSFDBK* low during the configuration period (CDSETUP* low)
CDSETUP*	37	I	TTL	**Card Setup:** Specifies that the host system is accessing the configuration (POS programmable option select) registers of the MCA adapter. (The adapter ID and configuration data is obtained by performing an I/O read cycle to the CL-PX2070. It contains POS 100, 101, and 102.)
IRQ*	45	O	TTL, 4	**Interrupt Request:** Specifies that the CL-PX2070 is requesting service from the host system
CDCHRDY	40	OD	TTL, 24	**Channel Ready:** When pulled low, specifies that the CL-PX2070 is not ready to complete the current host access cycle. The CL-PX2070 releases CDCHRDY to indicate that the current host access cycle should be completed

Signal	Pin	Type	Cell	Function *(cont.)*
CODS16*	39	OD	TTL, 24	**Card Data Size:** Specifies that the CL-PX2070 is able to respond as a 16 bit I/O data device for both read and write cycles.
CMD*	41	I	TTL	**Command:** Specifies that valid data is on bus AD[15:0] during a write cycle, and that the CL-PX2070 should place valid data on the bus during a read cycle
CORESET	42	I	TTL	**Reset:** Causes the CL-PX2070 to cease all activity and perform a hardware reset.
ADL*	33	I	TTL	**Address Latch:** Used to demultiplex the address from bus AD[15:0], and status from signals M/IO*, S1*, and S0*. The address and status must be valid during the LOW-to-HIGH transition

2.3 Processor Interface — Local Hardware Interface Mode

Signal	Pin	Type	Cell	Function
D[15:0]	48, 62, 65	I/O	TTL, 4	**Data Bus:** Bidirectional data bus that transfers video data between the host system and the CL-PX2070
RS[3:0]	34, 33, 44	I	TTL	**Register Select:** Specify the register address during a host access
BLAST*	43	O	TTL, 4	**Burst Last:** Specifies the last cycle of a DMA transfer
IOR*	35	I	TTL	**I/O Read Cycle:** Specifies an I/O read cycle
IOW*	36	I	TTL	**I/O Write Cycle:** Specifies an I/O write cycle
CS*	32	I	TTL	**Chip Select:** Specifies that the host system is accessing the CL-PX2070.
DMARQ*	38	O	TTL, 4	**DMA Request:** Specifies that the CL-PX2070 is requesting a DMA transfer.
DMACK*	37	I	TTL	**DMA Acknowledge:** Specifies that the host system is ready to perform a DMA transfer
IRQ*	45	O	TTL, 4	**Interrupt Request:** Specifies that the CL-PX2070 is requesting service from the host system
CHRDY*	40	OD	TTL, 24	**Channel Ready:** When asserted, indicates that the CL-PX2070 is not ready to complete the current host access cycle. The CL-PX2070 releases CHRDY to indicate that the current host access cycle should be completed
PCLK	41	I	TTL	**Processor Clock:** This input clock is used to synchronize the flow of data on bus D[15:0] during DMA data transfers

Signal	Pin	Type	Cell	Function *(cont.)*
RESET	42	I	TTL	**Reset:** This active high input signal causes the CL-PX2070 to cease all activity and perform a hardware reset
NC	39	N/A	N/A	**No Connect:** (must be left floating)

2.4 Graphics Overlay Interface

Signal	Pin	Type	Cell	Function
GPCLK	69	I	TTL	**Pixel Clock:** Clocks display output pixel data from the graphics controller
GVS	67	I	TTL	**Vertical Sync:** Identifies the start of the vertical sync interval. A vertical sync pulse is generated once every field time for interlaced data, and once every frame time for non interlaced data. Its polarity can be specified as either active high or active low
GHS	66	I	TTL	**Horizontal Sync:** Identifies the start of the horizontal sync interval. A horizontal sync pulse is generated once for each input line. Its polarity can be specified as either active high or active low
GBL	68	I	TTL	**Blanking:** Identifies the blanking interval. Its polarity can be specified as either active high or active low

2.5 Video Port 1 Interface

Signal	Pin	Type	Cell	Function
V1CLK	2	I	TTL	**Video Data Clock:** Clocks bidirectional video data on bus V1D[15:0]
V1D[15:0]	156, 153, 141, 138, 137	I/O	TTL, 4	**Video Data Bus:** Bidirectional data bus that transfers video data between the CL-PX2070 and an external device
V1VS	1	I/O	TTL, 4	**Vertical Sync:** Identifies the start of the vertical sync interval. A vertical sync pulse is generated once every field time for interlaced data, and once every frame time for non interlaced data. It can be specified as active-high or active-low
V1HS	160	I/O	TTL, 4	**Horizontal Sync:** Identifies the start of the horizontal sync interval. It can be specified as either active high or active low
V1BL	159	I/O	TTL, 4	**Horizontal/Composite Blanking:** Identifies the blanking interval. It can be specified as active high or active low

Signal	Pin	Type	Cell	Function (cont.)
V1PH	158	I	TTL, 4	**Phase:** Controls data qualification and duplexing of video data on bus V1D[15:0].
V1IEN*	157	O	TTL, 4	**Input Enable:** Specifies that the CL-PX2070 is not driving bus V1D[15:0]. V1IEN* can be used as a tristate control by an external buffer connected to bus V1D[15:0].

2.6 Video Port 2 Interface

Signal	Pin	Type	Cell	Function
V2CLK	29	I	TTL	**Video Data Clock:** Clocks bidirectional video data on bus V2D[15:0].
V2D[15:0]	3, 12, 14, 16, 19, 20, 22	I/O	TTL, 4	**Video Data Bus:** Transfers video data between the CL-PX2070 and an external device.
V2VS	27	I/O	TTL, 4	**Vertical Sync:** Identifies the start of the vertical sync interval. A vertical sync pulse is generated once every field time for interlaced data, and once every frame time for non-interlaced data. V2VS can be specified as active high or active-low.
V2HS	26	I/O	TTL, 4	**Horizontal Sync:** Identifies the start of the horizontal sync interval. V2HS can be specified as either active-high or active-low.
V2BI	25	I/O	TTL, 4	**Horizontal/Composite Blanking:** Identifies the blanking interval. V2BI can be specified as active-high or active-low.
V2PH	24	I	TTL	**Phase:** Controls data qualification and duplexing of video data on bus V2D[15:0].
V2IEN*	23	O	TTL, 4	**Input Enable:** Specifies that the CL-PX2070 is not driving bus V2D[15:0]. V2IEN* can be used as a tristate control by an external buffer connected to bus V2D[15:0].
STALLRQ*	31	I	TTL	**Stall Request:** Requests that the current transfer of video data on bus V2D[15:0] be suspended.
STALL*	30	O	TTL, 4	**Stall:** Specifies that the CL-PX2070 has suspended transferring data on bus V2D[15:0].

NOTE: Video input data mapping to the video data bus depends on the input-data format. See Section 3.3.2.1 for detailed information.

2.7 Frame Buffer Interface

Signal	Pin	Type	Cell	Function
FBD[31:0]	136, 128, 125, 109, 107, 105, 102, 101, 99	I/O	TTL, 4	**Data Bus:** Bidirectional data bus that transfers data between the CL-PX2070 and the Frame Buffer.
FBA[9:0]	98, 94, 92, 88	O	TTL, 8	**Address Bus:** Multiplexed output bus that specifies an address to the Frame Buffer. The row address is valid during the HIGH to LOW transition of signals RAS[1:0]*, and the column address is valid during the HIGH to LOW transition of signals CAS[1:0]*.
RAS[1:0]*	87, 86	O	TTL, 8	**Row Address Strobes:** Instruct the Frame Buffer to latch the row address from bus FBA[9:0] during the HIGH to LOW transition.
CAS[1:0]*	85, 84	O	TTL, 8	**Column Address Strobes:** Instruct the Frame Buffer to latch the column address from bus FBA[9:0] during the HIGH to LOW transition.
WE*	83	O	TTL, 12	**Write Enable:** Specifies a write cycle to the Frame Buffer.
DTE*	82	O	TTL, 12	**Data Transfer Enable:** Specifies a transfer cycle to the Frame Buffer (VRAMs only).
FRDY	81	I	TTL	**FIFO Ready:** (CL-PX2080 Mode) Specifies that the CL-PX2080 is ready to receive serial data from the Frame Buffer into its input FIFO.
ZC[3:0]	80, 77	O	TTL, 4	**Zoom Control Bus:** (CL-PX2080 Mode) Specifies to the CL-PX2080 the zoom factor to be used on the current data.
SBCLK	76	O	TTL, 8	**Serial Bus Clock:** Clocks serial data from the Frame Buffer (VRAMs only).
SOE[1:0]*	73, 72	O	TTL, 8	**VRAM Serial Port Output Enable:** Cause the Frame Buffer to assert the serial data port.
MCLK	71	I	TTL	**Memory Clock:** Synchronizes all Frame Buffer control signals.
FCLK	70	O	TTL, 8	**FIFO Write Clock:** (CL-PX2080 Mode) Clocks serial data into the CL-PX2080.

2.8 Power and Ground

Signal	Pin	Type	Cell	Function
VDD	18, 21, 46, 64, 75, 100, 103, 126, 140, 155	PWR	N/A	**+5 VDC for Digital Logic and Interface Buffers:** Each VDD pin must be connected directly to the VDD plane
VSS	13, 17, 28, 47, 63, 74, 93, 104, 108, 127, 139, 154	PWR	N/A	**Ground for Digital Logic and Interface Buffers:** Each VSS pin must be connected directly to the ground plane

3. FUNCTIONAL DESCRIPTION

The CL-PX2070 contains four major functional blocks - a core Video Processing Unit, which can process up to two external, bidirectional, real time video streams and a single external, bidirectional host video or graphic stream, and three related subsystems that perform complex interface functions. Figure 3-1 shows a functional block diagram of the CL-PX2070.

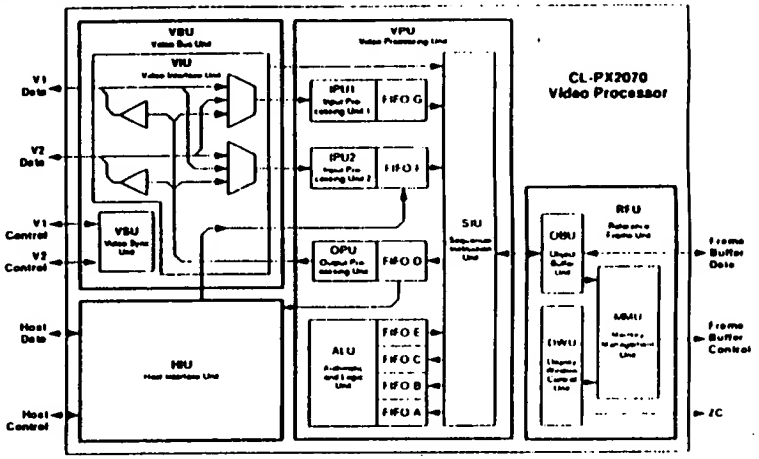


Figure 3-1. Functional Block Diagram

The *Host Interface Unit* (HIU) is a complete host interface that can be configured for ISA Bus, MCA Bus or local hardware interface operation. The HIU is the communication and data path between the host system and the CL-PX2070 based display system. See Section 3.1 on page 27 for additional information.

- The *Video Bus Unit* (VBU) is a highly programmable I/O path for video data. It contains two external digital video I/O ports, an internal input path from the HIU to the VPU, a sync unit, and a watchdog timer. See Section 3.2 on page 38 for additional information.
- The Video Processor Unit (VPU) provides field- or frame oriented video processing. It contains the master control register, a Sequencer Instruction Unit, two Input Processor Units, an Arithmetic and Logic Unit, and an Output Processor Unit. See Section 3.3 on page 46 for additional information.
- The Reference Frame Unit (RFU) manages the video data flow to and from the frame buffer. It contains an Object Buffer Unit, Display Window Control Unit, and Memory Management Unit. The RFU directly controls DRAM/VRAM devices, and defines up to eight graphics objects in multiple display windows. The innovative use of reference frames allows display windows to be resized and moved rapidly, with little CPU or software overhead. See Section 3.4 on page 70 for additional information.

Figure 3-2 shows the relationship of these blocks to each other, and the interconnection of the CL-PX2070 in a typical system

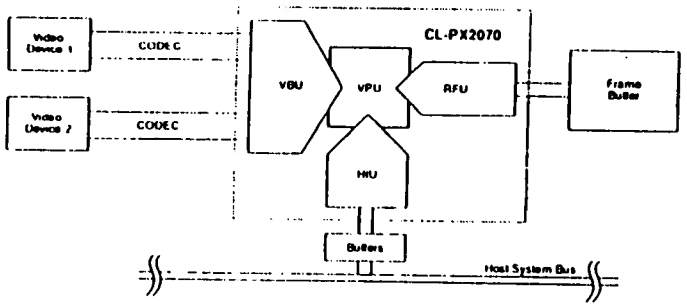


Figure 3-2. Typical CL-PX2070 System Interconnection

For additional detail concerning specific CL-PX2070 registers discussed in this section, refer to Section 4.

NOTE: Register names that contain lower case variables represent groups of registers with similar functions. For example, VIU_DPC1 represents either or both of the Datapath Control Registers — Register VIU_DPC1 (Datapath Control Field 1) and Register VIU_DPC2 (Datapath Control Field 2). Table 4-1 defines all variables used in this manner.

3.1 HIU: Host Interface Unit

The HIU, shown in Figure 3-1, provides the interface between the CL-PX2070 and the host system. It supports high speed DMA transfers of graphic or video data between the host system and the Frame Buffer, contains address decoding, Interface Registers, and related functions, and provides access to the CL-PX2070 Control Registers.

The HIU has two primary control functions:

- Hardware Configuration
- Register and Frame Buffer Interface.

3.1.1 Hardware Configuration

The HIU is central to the following hardware configurations.

- CL-PX2070 Configuration
- Host System Bus Configuration
- Frame Buffer Configuration
- Port Address Configuration.

3.1.1.1 CL-PX2070 Configuration

The CL-PX2070 is configured during power-up reset. The state of FBD[5:0] is written to the lower five bits of Register HIU_CSU at the falling edge of RESET. The FBD Signals are internally pulled up, which results in a 111 code (Local Mode) in HIU_CSU. (See Section 4.1.1 on page 82 for additional information.)

Table 3-1 shows the HIU_CSU bit-field assignments.

Table 3-1. Register Bit Assignments — External and Default (Local) Configurations

Signal(s)	HIU_CSU Field	Definition	Function (External Configuration)	Function (Default Configuration)
FBD[5:3]	HSB	Host System Bus	Specifies the host system connected to the CL-PX2070 to be ISA, MCA, or local hardware interface	Defaults to local hardware interface
FBD[2]		Reserved		
FBD[1]	FBT	Frame Buffer Type	Specifies the Frame Buffer memory to be DRAM or VRAM. This bit indicates the condition of FBD1 during reset, which is sometimes useful to application software. It has no effect on how the frame buffer interface functions.	Defaults to VRAM
FBD[0]	PAS	Port Address Select	Specifies whether the host system should select the primary or secondary I/O address map when accessing the CL-PX2070.	Field PAS is not active in local hardware interface mode. Address decode specified by Signals HS[2:1] (see Table 3-4).

External Configuration

External configuration is always used to configure ISA and MCA systems. The CL-PX2070 selects this configuration when any of FBD[5:3] are low. As shown in Figure 3-3, the CL-PX2070 reads the configuration dataset from Frame Buffer Data Bus Signals FBD[5:0]. These signals are latched into the LSB of Register HIU_CSU from an external tristate buffer at the falling edge of Signal RESET. Table 3-1 shows the bit to field mapping required for the data on these signals.

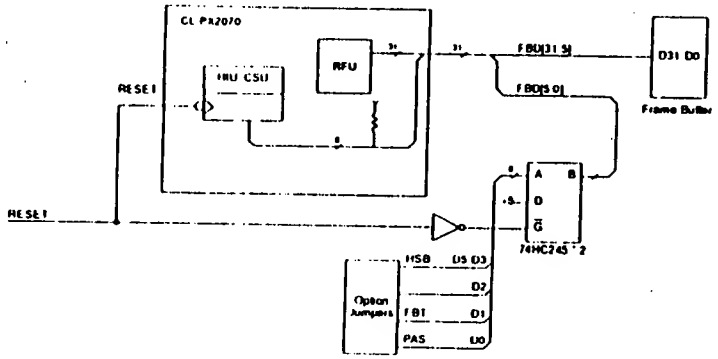


Figure 3-3. External Configuration

Default (Local) Configuration

The CL-PX2070 selects default (local) configuration when FBD[5:3] are high. This configuration, shown in Figure 3-4, causes the host system bus to default to local hardware interface mode. A fixed, default configuration of all bits high is loaded into the LSB of Register HIU_CSU, automatically providing the default configuration dataset. FBD[5:0] are internally pulled up.

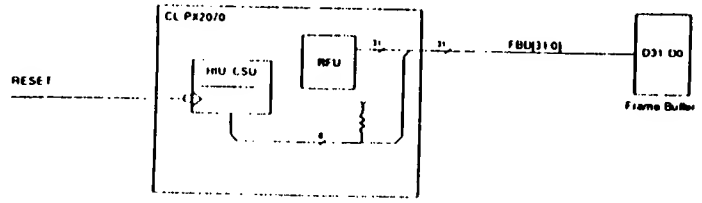


Figure 3-4. Default (Local) Configuration

3.1.1.2 Host System Bus Configuration

The HIU interfaces to two popular PC expansion buses:

- Industry Standard Architecture (ISA) Bus;
- Micro Channel Architecture (MCA) Bus.

For higher performance, the CL-PX2070 can also reside on the local hardware interface.

Table 3-2 highlights the primary features of the CL-PX2070 when operating in each of the three bus interfaces.

Table 3-2. CL-PX2070 System Interface Highlights

NOTE: Field HSB of Register HIU_CSU specifies which of the three interfaces is to be used.

	ISA Bus Interface	MCA Bus Interface	Local Hardware Interface
Interface	CL-PX2070 interfaces with the host system interface bus as shown in Figure 3-7		CL-PX2070 resides on the local hardware interface
Multiplex Support	Address and data buses are multiplexed. CL-PX2070 provides Signals DDIR and DEN* to support the required host system address/data multiplexing, and to provide bidirectional buffering of the host system data bus as shown in Figure 3-7		The data bus is not multiplexed
Address Decode	CL-PX2070 internally decodes the bus address during system I/O cycles. Table 3-4 lists the primary and secondary I/O address maps, selected during configuration, and the HIU Registers mapped to each		The host processor provides the decoded chip select Signal CS* to enable the CL-PX2070 host interface. Register select input Signals RS[3:1] can be connected to low order address lines to select the individual HIU Register. Table 3-4 shows the register select addresses
Register Access	CL-PX2070 supports standard register access cycles		
DMA Support	DMA through direct memory port	No DMA support	DMA through indexed memory port

The bus interface signals share a common set of I/O pins, as shown in Table 3-3. For a complete pin assignment table, refer to Section 1.2 on page 15.

Table 3-3. Host System Bus I/O Pins

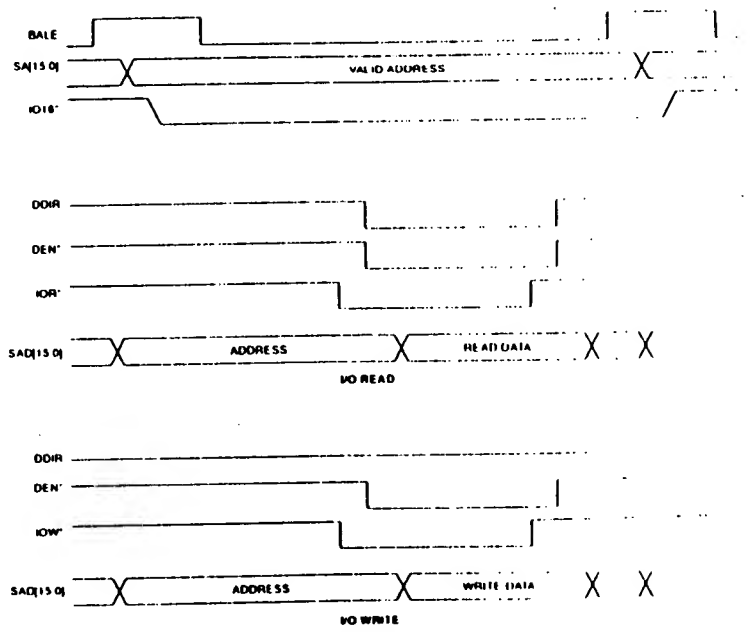
Pin	ISA Bus Interface		MCA Bus Interface		Local Hardware Interface	
32	AEN	I	M/IO*	I	CS*	I
33	NC	—	ADL*	I	RS[2]	I
34	AUXCS*[a]	I	CARDEN	I	RS[3]	I
35	IOR*	I	S1*	I	IOR*	I
36	IOW*	I	S0*	I	IOW*	I
37	DMACK*	I	CDSETUP*	I	DMACK*	I
38	DMARQ	O	CDSFDBK*	O	DMARQ*	O
39	IO16*	O	CDDS16*	O	NC	—
40	CHRDY	O	CDCHRDY	O	CHRDY*	O
41	BCLK	I	CMD*	I	PCLK	I
42	RESET	I	CDRESET	I	RESET	I
43	DDIR	O	DDIR	O	BLAST*	I
44	DEN*	O	DEN*	O	RS[1]	I
45	IRQ	O	IRQ*	O	IRQ*	O
48,62, 65	SAD[15:0]	I/O	AD[15:0]	I/O	D[15:0]	I/O

a. AUXCS* is used in AUX ISA mode. SAD[3:0] are used to address individual registers.

ISA Bus Interface

The CL-PX2070 interfaces with an ISA Bus using the pins listed in the Pin Assignment Table on page 15. The CL-PX2070 responds to I/O mapped bus cycles, including register access cycles and DMA cycles.

Register access cycles. The CL-PX2070 multiplexes the system address (SA[15:0]) and data (SD[15:0]) buses to Bus SAD[15:0] using external buffers controlled by Signals DDIR and DEN*. Figure 3-5 shows the signal relationship for the ISA Bus interface for register access cycles.



NOTE: BALE is shown only for reference — it is not used, ALE = 0.

Figure 3-5. ISA Bus Interface for Register Access Cycles

DMA cycles The CL-PX2070 supports high speed DMA cycles for bidirectional data transfer between the host system and the Frame Buffer. The CL-PX2070 must be programmed for DMA mode using Register HIU_OCS. Figure 3-6 shows the signals and general timing for the ISA Bus interface for DMA cycles.

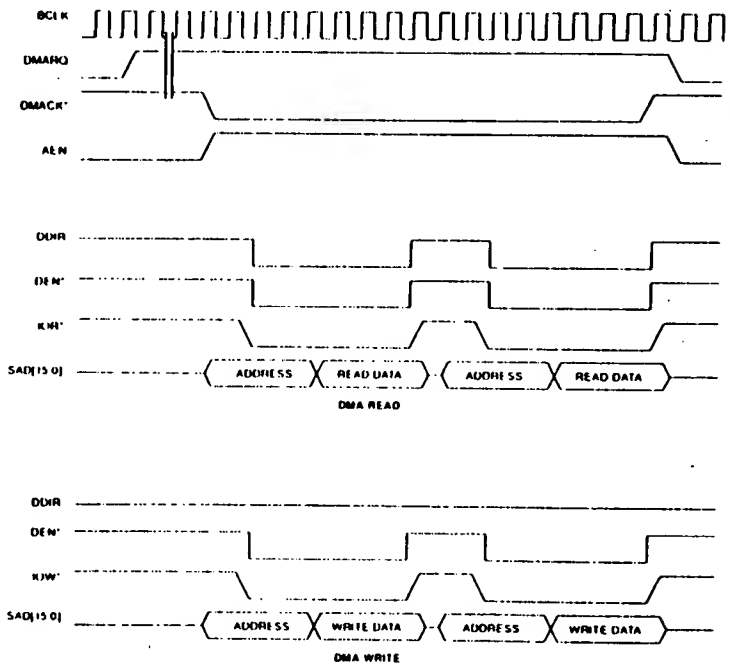


Figure 3-6. ISA Bus Interface for DMA Cycles

The lower eight bits of the CL-PX2070 address bus is multiplexed with the data bus. Figure 3-7 shows a method of interfacing the CL-PX2070 with the separate address and data buses of ISA. A similar circuit can be used to interface to the MCA Bus.

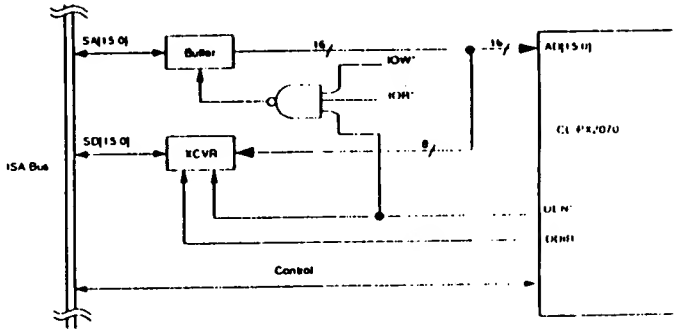


Figure 3-7. ISA and MCA Interface Address/Data Multiplexers

MCA Bus Interface

The CL-PX2070 interfaces with an MCA Bus using the pins shown in the Pin Assignment Table on page 15. The CL-PX2070 responds only to I/O-mapped bus cycles.

Register access cycles. The CL-PX2070 multiplexes the system address (A[15:0]) and data (D[15:0]) buses to Bus AD[15:0] using external buffers controlled by Signals DDIR and DEN*. Figure 3-8 shows the general timing for register access cycles. Refer to the detailed signal description on page 19 for the MCA Bus cycle decoding performed for Signals M/IO*, S0*, and S1*.

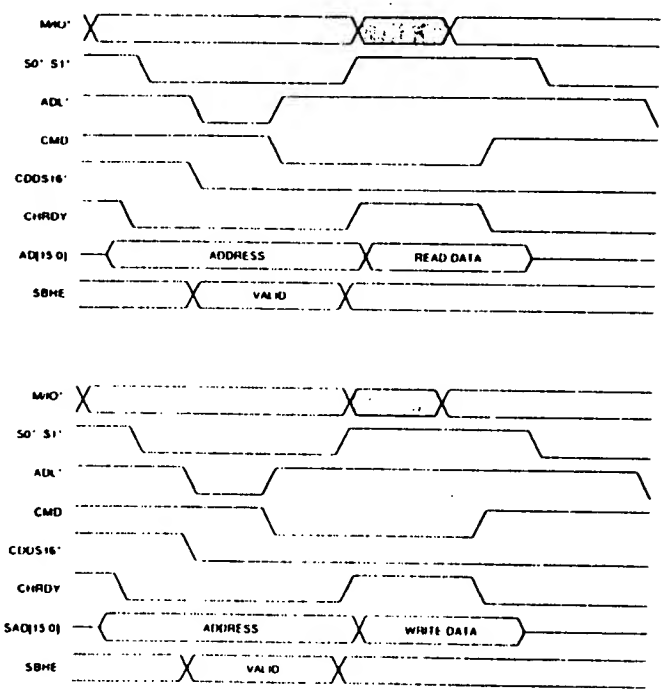


Figure 3-8. MCA Bus Interface for Register Access Cycles

Local Hardware Interface

The CL-PX2070 interfaces with a local processor using the pins shown in the Pin Assignment Table on page 16. The CL-PX2070 responds as an I/O device to register access cycles and DMA cycles, or may be used as a memory mapped device. Figure 3-9 shows the general timing for a register write, and Figure 3-10 shows the timing for a read cycle.

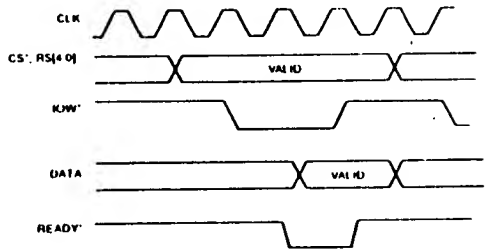


Figure 3-9. Local Hardware Interface Write Cycle

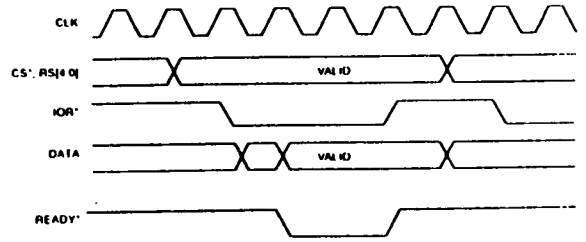


Figure 3-10. Read Timing (Local Hardware Interface)

DMA cycles The CL-PX2070 supports high speed DMA cycles for bidirectional data transfer between the host system and the Frame Buffer. The CL-PX2070 must be programmed for DMA mode using Register HIU_OCS. Figure 3-11 shows the signals and general timing for DMA cycles.

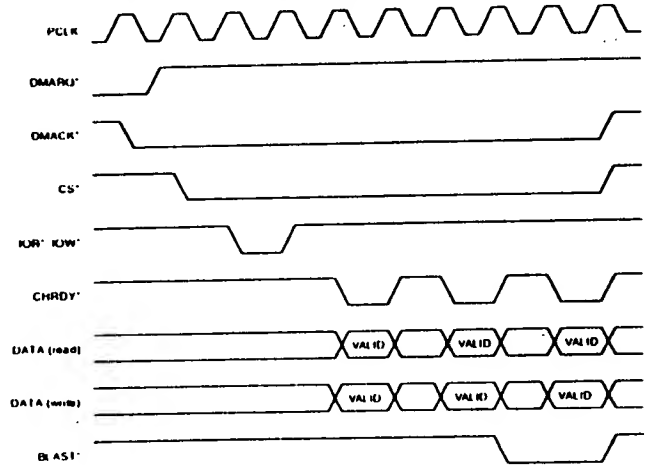


Figure 3-11. Local Hardware Interface DMA Cycles

3.1.1.3 Frame Buffer Configuration

No operational changes are required on the part of the CL-PX2070 between a design using a DRAM frame buffer and one using VRAM. The use of VRAM in a system based on the CL-PX2070 and the CL-PX2080 enables the full range of features. Field FBT of Register HIU_CSU is provided so that the firmware can determine the hardware configuration in which it is operating and adjust the available features accordingly. FBT defaults to VRAM.

3.1.1.4 Port Address Configuration

Table 3-4 shows the port address configurations for ISA, MCA, and Local Hardware Interface Modes. As shown in Table 3-1 on Page 27, field PAS of Register HIU_CSU specifies whether the host system uses the primary or secondary I/O address map when accessing the CL-PX2070 in ISA or MCA Modes (PAS is not active in Local Hardware Interface Mode).

Table 3-4. I/O Address Maps

	ISA and MCA Interfaces		Local H/W Interface		
Register	**Pri**	**Sec**	**RS[3:1]**	**Used By Registers**	
HIU_0	27C0h	0290h	0h	HIU_CSU HIU_DBG HIU_DRD	Configuration Setup (Read Only) Debug Control (Write Only) Debug Read (Read Only)
HIU_1	27C2h	0292h	1h	HIU_OCS HIU_IRQ	Operation Control/Status (Read/Write) Interrupt Status (Read Only)
HIU_2	27C4h	0294h	2h	HIU_RIN	Register Index (Read/Write)
HIU_3	27C6h	0296h	3h	HIU_RDT	Register Data Port (Read/Write)
HIU_4	27C8h	0298h	4h	HIU_MDT	Memory Data (Read/Write)

3.1.2 Register and Frame Buffer Interface

Regardless of whether the CL-PX2070 is operating in ISA, MCA, or local hardware interface mode, the CPU regards it as the five 16-bit registers defined in Table 3-4. These registers allow access to all CL-PX2070 data registers and to the Frame Buffer.

- *HIU_0 and HIU_1* control configuration and setup, overall operation, general status, and interrupt status.
- *HIU_2 and HIU_3* allow the host system to access the data registers
  - HIU_2 is the index, which points to the internal register to be accessed in the next I/O cycle.
  - HIU_3 is the data port.
- *HIU_4* is a frame buffer memory data port.

3.1.2.1 Internal Register Access

To read an internal register, the CPU writes the index address of the desired register into HIU_2 (HIU_RIN). It then reads HIU_3 (HIU_RDT), returning the value stored in the register specified by HIU_2. When autoincrement is enabled in HIU_3, the index value in HIU_2 increments after each access, allowing a group of contiguous registers to be loaded with a block transfer.

3.1.2.2 Accessing the Frame Buffer

To access the frame buffer, the CPU sets up an object buffer in the Reference Frame Unit for a block transfer, providing a pointer to a specific location in memory. A subsequent access to HIU_4 reads from or writes to the address associated with that buffer, taking advantage of the direct access that the HIU has to an input and an output FIFO within the VPU.

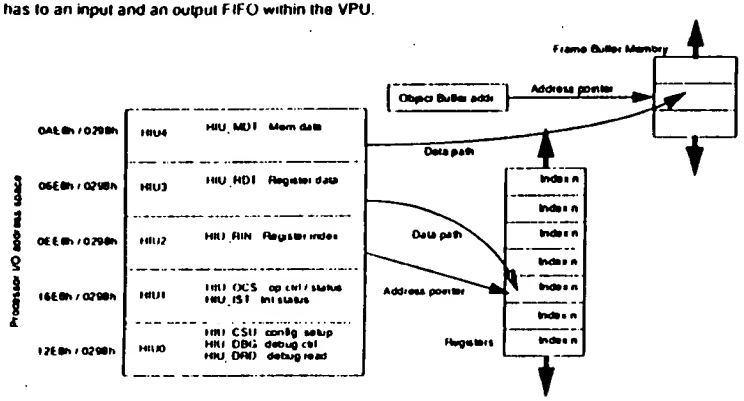


Figure 3-12. Register Access

For additional information on the Index and Data Registers, see also:

- Table 4-3 HIU Registers Accessed by the Register Data Port, p. 81
- Table 4-4 VBU Registers Accessed by the Register Data Port, p. 90
- Table 4-5 VPU Registers Accessed by the Register Data Port, p. 100
- Table 4-6. RFU registers Accessed by the Register Data Port, p. 136
- HIU_RIN, Register Index (Read/Write), page 87
- HIU_RDT, Register Data Port, page 88.

3.2 VBU: Video Bus Unit

The VBU, shown in Figure 3-1, manages the flow of video and graphic streams between the CL-PX2070 and up to three independent devices (including the host system). It also provides a data path between the CL-PX2070 and the host system for bidirectional graphic streams through the HIU.

The VBU provides two independent, real-time video I/O ports and contains two subunits, which are detailed in the following sections:

- VIU: Video Interface Unit. The VIU controls the flow of video data streams between the VPU and external video devices.
- VSU: Video Sync Unit. The VSU has independent sync signals for both video ports. Signal polarity

and direction are programmable.

In addition, three functional blocks within the Video Processing Unit (VPU) are closely related to the functionality of the VBU because of their I/O involvement. Each of these blocks and their associated FIFOs can be connected to either V1 or V2 under software control. For additional information concerning the VPU and its functional units, refer to Section 3.3 on page 46.

- *Input Processing Unit 1 (IPU1)* performs scaling, format conversion, window clipping, and color space conversion. FIFO G is IPU1's output. It feeds a data stream to the Sequencer Instruction Unit in the VPU. See Section 3.3.2 on page 50 for additional information.
- *Input Processing Unit 2 (IPU2)* performs window clipping only. FIFO F is IPU2's output. It feeds a data stream to the Sequencer Instruction Unit (SIU), also located in the VPU. See Section 3.3.3 on page 60 for additional information.
- *The Output Processor Unit (OPU)* receives data through FIFO D. The OPU can be connected back into IPU1 or IPU2. The OPU can act as sync slave, with outputs conforming to incoming video, if preferred. See Section 3.3.5 on page 68 for additional information.

Figure 3-13 illustrates the possible input and output paths (shown separately for simplicity) for video data. In addition to these paths, FIFO D can send to and FIFO F can receive from the HIU directly.

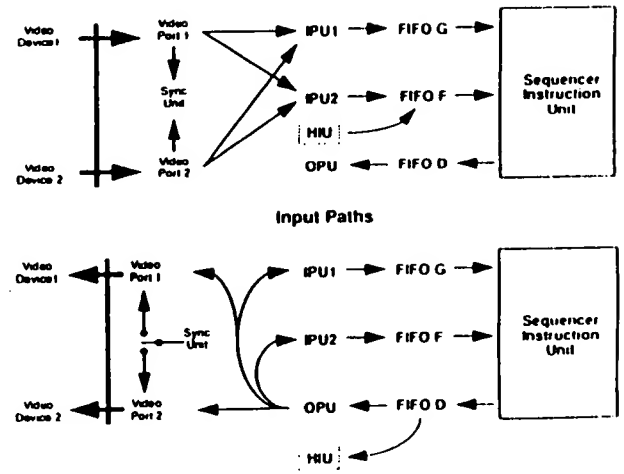


Figure 3-13. Possible Paths for Video Data

3.2.1 Video Ports V1 and V2

The VBU provides two 16 bit digital video ports — V1 and V2. Either port can be used with the VSU at any single point in time. V1 and V2 have the following characteristics:

- can be configured as input only, output only, or pixel- or field-duplexed I/O;
- provide programmable sync polarity;
- either port at one time can use the sync generator provided by the CL-PX2070;
- support the following formats:
  - 16-bit YCbCr, 12 bit YCbCr, 16 bit RGB, 8-bit RGB (input),
  - 16-bit YCbCr, 16 bit RGB, 8 bit RGB (output);
- V2 controls the video stream data flow between the CL-PX2070 and typical CODEC devices using Signals STALL* and STALLRQ*.

3.2.2 VIU: Video Interface Unit

The VIU controls the flow of video data streams between the VPU and external video devices. It specifies:

- the source and direction of video stream and sync control inputs,
- the field-toggling mode and field ID signals,
- the watchdog timer feature.

3.2.2.1 Video Stream and Sync Control Inputs

As shown in Figure 3-1, the VIU controls the flow of video streams through video ports V1 and V2 to all external devices, as well as the flow of internal streams. An input multiplexer directs one of two input streams or the output stream of the OPU to the input of the IPU1. A second input multiplexer directs one of two input streams or the output stream of the OPU to the input of the IPU2. A pair of buffers can output a stream from the output of the OPU to V1 or V2.

These functions are performed by the registers specified in Table 3-5.

Table 3-5. Video Stream and Sync Control Inputs — Control Registers

Register	Field	Function
VIU_MCRp	IOM	*Input/Output Mode* Specifies the direction of video stream data flow through video ports V1 and V2. Each port can be programmed as input only, output only, or as duplexed I/O under the control of Signal VpPH. NOTE: Each video port provides input enable Signal VpIEN* to control the three state buffers used in duplexed systems. If the port is programmed as input only, VpIEN* is asserted and held low. If the port is programmed as output only, VpIEN* is deasserted and held high. Two duplex modes are also provided. Depending on the control polarity specified for pixel phase input Signal VpPH in field IOM of Register VIU_MCRp, output Signal VpLEN* is driven to either match or be a complement of input Signal VpPH.
VIU_DPCI	IPU1DC	*IPU1 Datapath Control* Specifies the video stream and sync control inputs of the IPU1. IPU1 stream data and control sync can be driven by either V1 or V2. The input stream optionally can be qualified by Signal VpPH. When the OPU is specified as the source of the input stream, the sync references are provided by the internal sync generator. See also: VSU Video Sync Unit, page 43.
VIU_DPCI	IPU2DC	*IPU2 Datapath Control* Specifies the stream and sync control inputs of the IPU2. IPU2 stream data and control sync can be driven by either V1 or V2. The input stream optionally can be qualified by Signal VpPH. The stream data also can be driven from the host system through the HIU, bypassing the IPU2 and flowing directly to FIFO F. When the OPU is specified as the source of the input stream, the sync references are provided by the internal sync generator. See also: VSU Video Sync Unit, page 43.
VIU_DPCI	ODC	*ODC Datapath Control* Specifies the control sync source for the stream output from the OPU. A stream can also output to the host system by flowing directly from FIFO D to the HIU, bypassing the OPU.

3.2.2.2 Field Toggling and Field ID

The VPU subunits IPU1, IPU2, ALU, and OPU each contain parallel sets of registers (i.e., ALU Master Control Registers ALU_MCR1 and ALU_MCR2), allowing the CL-PX2070 to perform different operations on two independent, single-field video streams during a common frame time.

The SIU is the only VPU subunit that does not contain dual processors, but it does have a field toggle feature that distinguishes between the vertical sync pulses for each field and executes one of two different instruction sequences. This dual-field toggle feature requires a signal that specifies the set or field to be used.

The field synchronization signal is the master sync signal for the VPU; it is used to derive two signals:

- *Field ID Signal FID.* The state of this internal signal (in interlaced mode) is determined by the sync signals. In non-interlaced mode this value remains at 0. FID specifies the register set that is to be used in the IPU1, IPU2, ALU, and OPU; it is shown in Figure 3-16, Figure 3-17, and Figure 3-24.
- *Field Toggle Signal.* This signal determines whether the SIU selects field 1 or field 2.
  See also: SIU: Sequencer Instruction Unit, page 46.
- These functions are performed by the register specified in Table 3-6.

Table 3-6. Field Toggling and Field ID — Control Registers

Register	Field	Function
VIU_WDT	MFTS	Master Field Toggle Select. Specifies whether the VPU is to determine its field synchronization signal from the vertical sync pulse on: • video port V1, • video port V2, or • the watchdog timer (the watchdog timer can supply a signal when processing streams without sync controls). • software command. See Section 4.2.1.3 on page 94.

3.2.2.3 Watchdog Timer

The VIU's watchdog timer can generate a watchdog timer signal to detect a loss-of-sync condition, or it can emulate sync references for streams which have no sync (such as graphic stream data to or from the host system).

Its functions are performed by the register fields specified in Table 3-7.

Table 3-7. Watchdog Timer — Control Registers

Register	Field	Function
VIU_WDT	WTE	Watchdog Timer Enable. Enables or disables the operation of the watchdog timer. Disabling and then re-enabling resets the counter to the programmed value.
VIU_WDT	TMOUT	Timeout Interval. Specifies the 10-bit timeout period count of the watchdog timer. This count is based on the input memory clock Signal MCLK. MCLK is prescaled by a factor of 49,152 (3 * 214) for use by the timeout counter. Assuming a 60 MHz value for Signal MCLK, the timeout range available would be from 0.82 ms (TMOUT count = 1) to 838 ms (TMOUT count = 1023).

3.2.3 VSU: Video Sync Unit

The Video Sync Unit (VSU) has independent sync signals for both video ports. Signal polarity and direction are programmable.

The VSU implements identical, independent video reference signals for each video port:

- *VpVS (vertical/composite sync)* — bidirectional video sync signal that identifies the beginning of a field (interlaced stream) or frame (non-interlaced stream);
- *VpHS (horizontal sync)* — bidirectional video sync signal that identifies the beginning of a line;
- *VpHB (horizontal/composite blanking)* — input or output signal that specifies the horizontal/composite blanking interval.

Each video port implements independent control of sync polarity for each of these signals. Master control Registers VIU_MCRp provide matching fields that specify input and output sync modes, as shown in Table 3-8.

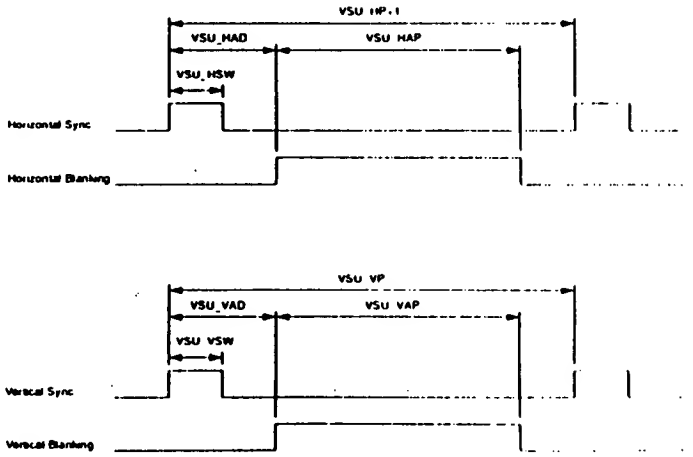
Table 3-8. Input and Output Sync Modes — Control Registers

Registers	Fields	Function
Output Sync Modes		
VIU_MCRp	OVSP	Output Video Vertical Sync Polarity. Specifies polarity of vertical sync signals V1VS (VIU_MCR1) and V2VS (VIU_MCR2) when signals are used as output.
VIU_MCRp	OHSP	Output Video Horizontal Sync Polarity. Specifies polarity of horizontal sync signals V1HS (VIU_MCR1) and V2HS (VIU_MCR2) when signals are used as output.
VIU_MCRp	OBP	Output Video Blank Polarity. Specifies polarity of horizontal/composite blanking signals V1BL (VIU_MCR1) and V2BL (VIU_MCR2) when signals are used as output.
VIU_MCRp	OBT	Output Video Blank Type. Specifies horizontal/composite blanking signals V1BL (VIU_MCR1) and V2BL (VIU_MCR2) to be either Hblank or Cblank when signals are used as output.
Input Sync Modes		
VIU_MCRp	IVSP	Input Video Vertical Sync Polarity. Specifies polarity of vertical sync signals V1VS (VIU_MCR1) and V2VS (VIU_MCR2) when signals are used as input.
VIU_MCRp	IHSP	Input Video Horizontal Sync Polarity. Specifies polarity of horizontal sync signals V1HS (VIU_MCR1) and V2HS (VIU_MCR2) when signals are used as input.
VIU_MCRp	IBP	Input Video Blank Polarity. Specifies polarity of horizontal/composite blanking signals V1BL (VIU_MCR1) and V2BL (VIU_MCR2) when signals are used as input.
VIU_MCRp	IBT	Input Video Blank Type. Specifies horizontal/composite blanking signals V1BL (VIU_MCR1) and V2BL (VIU_MCR2) to be either Hblank or Cblank when signals are used as input.

The VSU implements an internal sync generator to provide the horizontal and vertical references, listed in Table 3-9, when the CL-PX2070 is programmed as a sync master (see Figure 3-14). The references can then be directed to V1, V2, IPU1, or IPU2. Fields IPU1DC and IPU2DC in Register VIU_DPCf specify the horizontal timebase reference for the internal sync generator as either MCLK/3 or as MCLK/6 when the OPU sources the data stream to IPU1 or IPU2. The OPU must always be programmed with the VSU internal syncs if it outputs to the IPU1 or IPU2 data paths.

Table 3-9. Horizontal and Vertical References — Control Registers

Register	Field	Function
Horizontal References		
VSU_HP	—	Horizontal Period. Specifies the total number of horizontal timebase clock periods in the horizontal interval. NOTE: The actual period is the number entered in this field *plus one*
VSU_HSW	—	Horizontal Sync Width. Specifies the number of horizontal timebase clock periods for the interval of the horizontal sync pulse.
VSU_HAD	—	Horizontal Active Delay. Specifies the number of horizontal timebase clock periods for the interval between the beginning of the horizontal sync pulse and the beginning of active pixel period.
VSU_HAP	—	Horizontal Active Pixels. Specifies the number of horizontal timebase clock periods for the interval of active pixels per line
Vertical References		
VSU_VP	—	Vertical Period. Specifies the total number of horizontal sync intervals in the vertical interval
VSU_VSW	—	Vertical Sync Width. Specifies the number of horizontal sync intervals for the interval of the vertical sync pulse
VSU_VAD	—	Vertical Active Delay. Specifies the number of horizontal sync intervals for the interval between the beginning of the vertical sync pulse and the beginning of active line period
VSU_VAP	—	Vertical Active Pixels. Specifies the number of horizontal sync intervals for the interval of active rows per field (interlaced) or frame (non-interlaced)



NOTE: In this example, the VIU_MCR sync polarity bits are programmed as 1, for active high sync.

Figure 3-14. Programmability of the Internal Sync Generator

3.3 VPU: Video Processor Unit

The VPU, shown in Figure 3-1, provides field oriented video processing. It can simultaneously process up to two external, bidirectional real time video streams and a single external, bidirectional host video or graphic stream.

The VPU contains the Master Control Register VPU_MCR (described in section 4.3.1, page 105), and five subunits, each of which is detailed in the following subsections:

- SIU: Sequencer Instruction Unit
- IPU1: Input Processor Unit 1
- IPU2: Input Processor Unit 2
- ALU: Arithmetic and Logic Unit
- OPU: Output Processor Unit.

IPU1, IPU2, and the OPU provide the video data paths between video ports V1 and V2 and the SIU. The SIU moves data between the hardware resources. The ALU can operate on pixels logically or arithmetically, replace a pixel or one of its component values with a constant, and decode and/or encode pixels tags.

3.3.1 SIU: Sequencer Instruction Unit

The SIU is a special purpose microcontroller that moves pixel data between the hardware resources under the control of instruction sequences stored in the SIM.

The SIU resembles a short software loop made of conditional instructions. Each instruction causes data to move between the components listed in Table 3-10, and specifies:

- the source of the video information,
- conditions for execution, destination, and
- the location of the next instruction.

Possible sources and destinations are object buffers and FIFOs A-G.

Table 3-10. CL-PX2070 FIFOs

Component	Dedicated FIFO	FIFO Depth
IPU1 Input Processor Unit 1	FIFO G	128 bytes
IPU2 Input Processor Unit 2	FIFO F	128 bytes
ALU Arithmetic and Logic Unit	FIFOs A, B, C, E	64 bytes
OPU Output Processor Unit	FIFO D	128 bytes
OBU Object Buffer Unit	N/A	N/A

Figure 3-15 is an overview of SIU instruction flow.

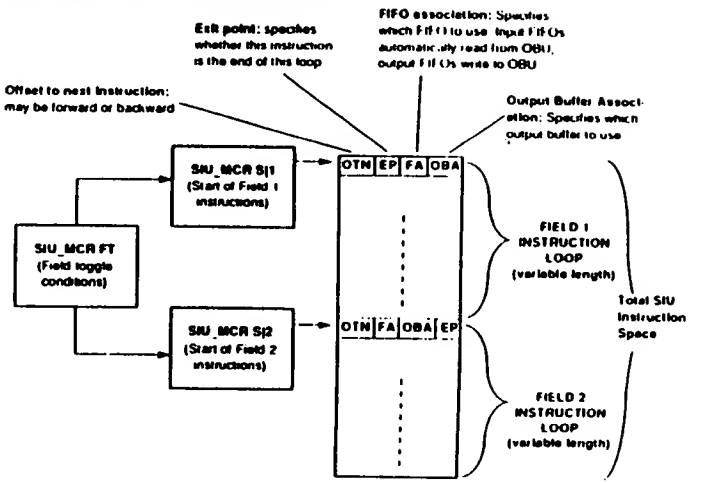


Figure 3-15. SIU Instruction Flow

The SIU can execute SIM instructions much faster than the stream rates of typical video data. Therefore, the instructions are conditional. At any given time, the FIFO associated with the current instruction may or may not be ready to source or receive data. If it is not ready, the SIU skips the instruction and continues with the next until an instruction is found which can be executed.

Internal OBU controls allow a stream being written from an output FIFO to an object buffer to be simultaneously copied to an input FIFO, reducing data-path traffic in recursive processing operations.

The following sections detail the major components and functions of the SIU.

- Programming the SIU
- Master Control Register SIU_MCR
- Sequencer Instruction Memory SIUs_SIM
- Accessing FIFO Control/Status Indicators.

3.3.1.1 *Programming the SIU*

The SIU can be programmed for all the following operations:

- a single instruction sequence loop used to process
  - a single non-interlaced stream, or
  - one or both fields of an interlaced stream.

- two instruction sequence loops used to process ..
  - — two different, non-interlaced streams,
  - — a single non-interlaced stream and a single field from an interlaced stream,
  - — both fields of a single interlaced stream, or
  - — a single field each from two different, interlaced streams;
- multiple instruction sequences used to process...
  - — an arbitrary number of streams.

To program the SIU, determine the path of the video stream and plan the desired conversions. Then allocate the various hardware resources and configure them accordingly.

The SIU can be programmed to be field time controlled. That is, it can execute one sequence loop in the even field time, and another sequence loop in the odd field time. (See also: Field Toggling and Field ID, page 42)

Because the SIU is field based, the controlling software application must specify the source of the vertical sync pulse that performs the field toggle, and whether other stream processing is to be performed at the same time. Field MFTS of Register VIU_WDT specifies the source of the sync signal used for the field toggle, as shown in Table 3-6.

3.3.1.2 Master Control Register SIU_MCR

Master Control Register SIU_MCR directs entry points into the SIU for sequencer cycling. It performs the functions specified in Table 3-11.

Table 3-11. Master Control Register SIU_MCR

Register	Field	Function
SIU_MCR	SI1	**Start Index 1.** Specifies a start instruction index for Field Time 1. The value in SI1 is the index in the SIM of the first instruction executed in Field Time 1.
SIU_MCR	SI2	**Start Index 2.** Specifies a start instruction index for Field Time 2. The value in SI2 is the index in the SIM of the first instruction executed in Field Time 2.
SIU_MCR	FT	**Field Toggle.** Specifies four modes of field timing sync. • No field toggle (SI1 is used, SI2 is ignored). • SI1 and SI2 toggle on vertical sync, no field association. • Field 1 is associated to SI1, and fields 1 and 2 toggle on vertical sync • Field 2 is associated to SI2, and fields 1 and 2 toggle on vertical sync.
SIU_MCR	SE	**Sequencer Enable.** Halts the SIU, or specifies that the SIU start on field SI1 or SI2

3.3.1.3 Sequencer Instruction Memory SIUs_SIM

Sequencer Instruction Memory SIUs_SIM is a register file that stores the sequence instruction. It contains 32 identical 16-bit registers, indexed from 0 to 31 (SIM[31:0]). Each register stores one instruction that contains four fields, as described in Table 3-12.

Table 3-12. SIUs_SIM Instruction Fields

Register	Field	Function
SIUs_SIM	OTN	**Offset to Next Instruction.** Specifies the signed, 5 bit offset to the next instruction. This value can be positive or negative (to implement a simple loop). and is added to the current instruction index to generate the index of the next instruction to execute. For example, if SIM[8] is the current instruction and has an OTN value of -3, SIM[5] will be the next instruction executed.
SIUs_SIM	EP	**Exit Point.** Specifies that the current instruction is the exit point of the current sequence loop.
SIUs_SIM	FA	**FIFO Association.** Specifies the source or destination FIFO for the current instruction. (Each SIM instruction associates a FIFO to an object buffer, thus implying a direction. For example, associating an output FIFO to an object buffer implies a write operation from the FIFO to the object buffer.)
SIUs_SIM	OBA	**Object Buffer Association.** Specifies the corresponding destination or source object buffer for the current instruction.

3.3.1.4 Accessing FIFO Control/Status Indicators

Each FIFO has four flags which the controlling software application can access through the two SIU Registers described in Table 3-13.

Table 3-13. Accessing FIFO Control/Status Indicators — Control Registers

Register	Field	Function
SIU_FOU	—	**FIFO Overflow/Underflow.** Provides access to the overflow and underflow flags.
SIU_FCS	—	**FIFO Control/Status.** Returns the current full and empty status flags. Writing to any of the FIFO empty fields (FxE) halts and resets the corresponding FIFO. See also: SIU_FCS: FIFO Control/Status, page 124. NOTE: Register SIU_FCS is a special read/write register. On read, the status flags are returned. During a write, only the FxE fields are used to reset the FIFO. The reset values cannot be read back, so the controlling software application must retain a copy.

3.3.2 IPU1: Input Processor Unit 1

The IPU1, shown in Figure 3-16, prepares an input video stream for ALU processing and/or storage in the Frame Buffer, then outputs the prepared stream through FIFO G to the Frame Buffer Data Bus. Its video processing features include YCbCr and RGB input stream format conversion, color space conversion, programmable data tagging, three channel lookup table operations, horizontal prescaling, window clipping, horizontal and vertical scaling, and output stream format conversion.

The IPU1 has two Master Control Registers (IPU1_MCR1 and IPU1_MCR2), allowing the IPU1 to perform different operations on two independent, single-field video streams during a common frame time. Field ID Signal FID, shown in Figure 3-16, determines the register set to be used. See also: Field Toggling and Field ID, page 42.

The IPU1 contains seven subunits, each of which is detailed in the following paragraphs:

- 6Input Format Converter and Chrominance Interpolator
- Input Tag Unit
- Color Space Converter
- LUT RAM
- X Prescaler
- Window Clipping and XY Scaler
- Output Format Converter Unit.

This section also describes the IPU1 Interrupt Request Unit.

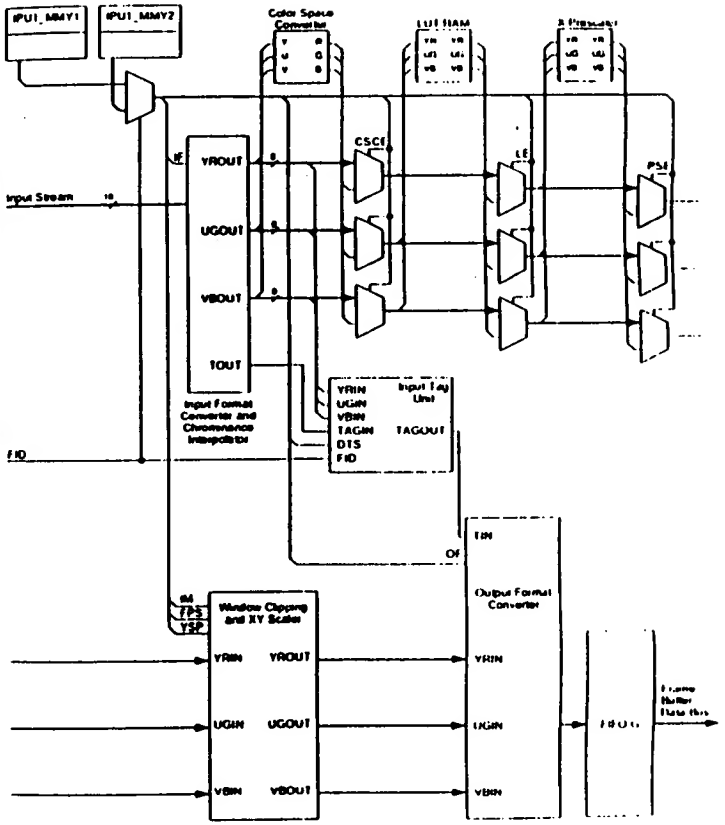


Figure 3-16. IPU1: Input Processor Unit 1

3.3.2.1 Input Format Converter and Chrominance Interpolator

The Input Format Converter and Chrominance Interpolator, shown in Figure 3-16, has two functions:

- The *Input Format Converter* operates on external and internal streams. It produces three 8-bit and one 1-bit tag buses that are used exclusively by the other IPU1 subunits. These tag buses do not appear outside the IPU1.
- The *Chrominance Interpolator*

Input Format Converter

The Input Format Converter demultiplexes 16-bit 4:2:2 or 12-bit 4:1:1 YCbCr video data into the non-multiplexed format used by IPU1 (8-bit YR, UG, and VB buses with a 1-bit tag, as shown in Figure 3-16). The Input Format Converter accepts as input:

- the YCbCr video input stream formats defined in Table 3-14,
- the 16-bit RGB video input stream formats defined in Table 3-15, and
- the pseudocolor video input stream format defined in Table 3-16.

These formats are specified by field IF in Registers IPU1_MCRf for each field time.

NOTE: These specified input formats *do not* imply that the Input Format Converter performs color space conversion. A specified YCbCr format implies that the stream input for processing will be in YCbCr format. A specified RGB format implies that the stream input for processing will be in RGB format. The controlling software application must ensure that the desired processing is compatible with input video stream.

Table 3-14. YCbCr Video Input Stream Formats

NOTE: The Video Input Stream Formats in this table are shown for four consecutive VpCLK clocks C_1-C_4.

4:2:2 YCbCr Non-Tagged					4:2:2 YCbCr Tagged					4:1:1 YCbCr Non-Tagged				
VpD	CLK$_1$	CLK$_2$	CLK$_3$	CLK$_4$	VpD	CLK$_1$	CLK$_2$	CLK$_3$	CLK$_4$	VpD	CLK$_1$	CLK$_2$	CLK$_3$	CLK$_4$
VpD15	Y7$_1$	Y7$_2$	Y7$_3$	Y7$_4$	VpD15	Y7$_1$	Y7$_2$	Y7$_3$	Y7$_4$	VpD15	Y7$_1$	Y7$_2$	Y7$_3$	Y7$_4$
VpD14	Y6$_1$	Y6$_2$	Y6$_3$	Y6$_4$	VpD14	Y6$_1$	Y6$_2$	Y6$_3$	Y6$_4$	VpD14	Y6$_1$	Y6$_2$	Y6$_3$	Y6$_4$
VpD13	Y5$_1$	Y5$_2$	Y5$_3$	Y5$_4$	VpD13	Y5$_1$	Y5$_2$	Y5$_3$	Y5$_4$	VpD13	Y5$_1$	Y5$_2$	Y5$_3$	Y5$_4$
VpD12	Y4$_1$	Y4$_2$	Y4$_3$	Y4$_4$	VpD12	Y4$_1$	Y4$_2$	Y4$_3$	Y4$_4$	VpD12	Y4$_1$	Y4$_2$	Y4$_3$	Y4$_4$
VpD11	Y3$_1$	Y3$_2$	Y3$_3$	Y3$_4$	VpD11	Y3$_1$	Y3$_2$	Y3$_3$	Y3$_4$	VpD11	Y3$_1$	Y3$_2$	Y3$_3$	Y3$_4$
VpD10	Y2$_1$	Y2$_2$	Y2$_3$	Y2$_4$	VpD10	Y2$_1$	Y2$_2$	Y2$_3$	Y2$_4$	VpD10	Y2$_1$	Y2$_2$	Y2$_3$	Y2$_4$
VpD9	Y1$_1$	Y1$_2$	Y1$_3$	Y1$_4$	VpD9	Y1$_1$	Y1$_2$	Y1$_3$	Y1$_4$	VpD9	Y1$_1$	Y1$_2$	Y1$_3$	Y1$_4$
VpD8	Y0$_1$	Y0$_2$	Y0$_3$	Y0$_4$	VpD8	Y0$_1$	Y0$_2$	Y0$_3$	Y0$_4$	VpD8	Y0$_1$	Y0$_2$	Y0$_3$	Y0$_4$
VpD7	U7$_1$	V7$_1$	U7$_3$	V7$_3$	VpD7	U7$_1$	V7$_1$	U7$_3$	V7$_3$	VpD7	U7$_1$	U5$_1$	U3$_1$	U1$_1$
VpD6	U6$_1$	V6$_1$	U6$_3$	V6$_3$	VpD6	U6$_1$	V6$_1$	U6$_3$	V6$_3$	VpD6	U6$_1$	U4$_1$	U2$_1$	U0$_1$
VpD5	U5$_1$	V5$_1$	U5$_3$	V5$_3$	VpD5	U5$_1$	V5$_1$	U5$_3$	V5$_3$	VpD5	V7$_1$	V5$_1$	V3$_1$	V1$_1$
VpD4	U4$_1$	V4$_1$	U4$_3$	V4$_3$	VpD4	U4$_1$	V4$_1$	U4$_3$	V4$_3$	VpD4	V6$_1$	V4$_1$	V2$_1$	V0$_1$
VpD3	U3$_1$	V3$_1$	U3$_3$	V3$_3$	VpD3	U3$_1$	V3$_1$	U3$_3$	V3$_3$	VpD3	—	—	—	—
VpD2	U2$_1$	V2$_1$	U2$_3$	V2$_3$	VpD2	U2$_1$	V2$_1$	U2$_3$	V2$_3$	VpD2	—	—	—	—
VpD1	U1$_1$	V1$_1$	U1$_3$	V1$_3$	VpD1	U1$_1$	V1$_1$	U1$_3$	V1$_3$	VpD1	—	—	—	—
VpD0	U0$_1$	V0$_1$	U0$_3$	V0$_3$	VpD0	T$_1$	T$_2$	T$_3$	T$_4$	VpD0	—	—	—	—

Table 3-15. 16-bit RGB Video Input Stream Formats

5:6:5 RGB Non-Tagged					5:5:5 RGB Non-Tagged					5:5:5 RGB Tagged				
VpD	CLK$_1$	CLK$_2$	CLK$_3$	CLK$_4$	VpD	CLK$_1$	CLK$_2$	CLK$_3$	CLK$_4$	VpD	CLK$_1$	CLK$_2$	CLK$_3$	CLK$_4$
VpD15	R7$_1$	R7$_2$	R7$_3$	R7$_4$	VpD15	—	—	—	—	VpD15	T$_1$	T$_2$	T$_3$	T$_4$
VpD14	R6$_1$	R6$_2$	R6$_3$	R6$_4$	VpD14	R7$_1$	R7$_2$	R7$_3$	R7$_4$	VpD14	R7$_1$	R7$_2$	R7$_3$	R7$_4$
VpD13	R5$_1$	R5$_2$	R5$_3$	R5$_4$	VpD13	R6$_1$	R6$_2$	R6$_3$	R6$_4$	VpD13	R6$_1$	R6$_2$	R6$_3$	R6$_4$
VpD12	R4$_1$	R4$_2$	R4$_3$	R4$_4$	VpD12	R5$_1$	R5$_2$	R5$_3$	R5$_4$	VpD12	R5$_1$	R5$_2$	R5$_3$	R5$_4$
VpD11	R3$_1$	R3$_2$	R3$_3$	R3$_4$	VpD11	R4$_1$	R4$_2$	R4$_3$	R4$_4$	VpD11	R4$_1$	R4$_2$	R4$_3$	R4$_4$
VpD10	G7$_1$	G7$_2$	G7$_3$	G7$_4$	VpD10	R3$_1$	R3$_2$	R3$_3$	R3$_4$	VpD10	R3$_1$	R3$_2$	R3$_3$	R3$_4$
VpD9	G6$_1$	G6$_2$	G6$_3$	G6$_4$	VpD9	G7$_1$	G7$_2$	G7$_3$	G7$_4$	VpD9	G7$_1$	G7$_2$	G7$_3$	G7$_4$
VpD8	G5$_1$	G5$_2$	G5$_3$	G5$_4$	VpD8	G6$_1$	G6$_2$	G6$_3$	G6$_4$	VpD8	G6$_1$	G6$_2$	G6$_3$	G6$_4$
VpD7	G4$_1$	G4$_2$	G4$_3$	G4$_4$	VpD7	G5$_1$	G5$_2$	G5$_3$	G5$_4$	VpD7	G5$_1$	G5$_2$	G5$_3$	G5$_4$
VpD6	G3$_1$	G3$_2$	G3$_3$	G3$_4$	VpD6	G4$_1$	G4$_2$	G4$_3$	G4$_4$	VpD6	G4$_1$	G4$_2$	G4$_3$	G4$_4$
VpD5	G2$_1$	G2$_2$	G2$_3$	G2$_4$	VpD5	G3$_1$	G3$_2$	G3$_3$	G3$_4$	VpD5	G3$_1$	G3$_2$	G3$_3$	G3$_4$
VpD4	B7$_1$	B7$_2$	B7$_3$	B7$_4$	VpD4	B7$_1$	B7$_2$	B7$_3$	B7$_4$	VpD4	B7$_1$	B7$_2$	B7$_3$	B7$_4$
VpD3	B6$_1$	B6$_2$	B6$_3$	B6$_4$	VpD3	B6$_1$	B6$_2$	B6$_3$	B6$_4$	VpD3	B6$_1$	B6$_2$	B6$_3$	B6$_4$
VpD2	B5$_1$	B5$_2$	B5$_3$	B5$_4$	VpD2	B5$_1$	B5$_2$	B5$_3$	B5$_4$	VpD2	B5$_1$	B5$_2$	B5$_3$	B5$_4$
VpD1	B4$_1$	B4$_2$	B4$_3$	B4$_4$	VpD1	B4$_1$	B4$_2$	B4$_3$	B4$_4$	VpD1	B4$_1$	B4$_2$	B4$_3$	B4$_4$
VpD0	B3$_1$	B3$_2$	B3$_3$	B3$_4$	VpD0	B3$_1$	B3$_2$	B3$_3$	B3$_4$	VpD0	B3$_1$	B3$_2$	B3$_3$	B3$_4$

Table 3-16. 8-bit Pseudocolor Video Input Stream Formats

8-bit Pseudocolor Non-Tagged (Multiplexed a,b)	
VpD	C$_{Lk1}$
VpD15	P7
VpD14	P6
VpD13	P5
VpD12	P4
VpD11	P3
VpD10	P2
VpD9	P1
VpD8	P0
VpD7	—
VpD6	—
VpD5	—
VpD4	—
VpD3	—
VpD2	—
VpD1	—
VpD0	—

Chrominance Interpolator

The Chrominance Interpolator accepts the following input data formats.

- *4 2 2 YCbCr*. When 4 2 2 YCbCr data is input, the Chrominance Interpolator increases the sample rate of the Cb and Cr channels with a low-pass filter function to produce the equivalent of a 4:4:4 YCbCr stream.
- *4 1 1 YCbCr*. The Chrominance Interpolator first converts 4:1:1 YCbCr data into a 4:2:2 YCbCr stream, then outputs it to the chrominance filter for processing (this process is automatic when 4:1:1 YCbCr data is specified). All results are rounded to 8 bits. Values less than 0 are set to 0, and values greater than 255 are set to 255.
- *8 bit pseudocolor*. When the 8 bit pseudocolor input data format is specified, the Input Format Converter replicates the input 8 bit pixel value to all three 8-bit channels (primarily for the use of the Color Space Converter in producing 24 bit RGB or YCbCr data).

3.3.2.2 Input Tag Unit

The Input Tag Unit, shown in Figure 3-17, implements independent YCbCr chroma key tagging on the input data stream. A complete register set (IPU1_MCR1 through IPU1_MMV1, IPU1_MCR2 through IPU1_MMV2, as shown in Table 4-6) is provided for each field time to independently tag fields 1 and 2.

Field ODT in Registers IPU1_MCR1 specifies four tagging modes:

- existing input stream tag (if any) remains unchanged,
- input stream is tagged with the ID of the current field (0 = field 1, 1 = field 2),
- input stream is tagged with the output of the chroma key multiplexer,
- input stream is tagged with the inverse of the chroma key multiplexer.

Three independent, identical chroma key comparator circuits -- one for each of three input channels — discriminate pixel values found between the programmable 8 bit minimum and maximum values defined in Registers IPU1_MMV1, IPU1_MMU1, and IPU1_MMV1. As shown in Figure 3-17, the output of each comparator circuit selects one of the four inputs to the chroma key multiplexer.

NOTE: The inputs of the comparator circuits are also programmable using Registers IPU1_KFC1. This flexibility allows the input stream to be tagged according to a pixel data value for any of the three channels independently, or for any independent combination of pixel values found on the three channels.

3.3.2.3 Color Space Converter

The Color Space Converter transforms YCbCr pixel values into the equivalent RGB pixel values using the functions specified in *The International Telecommunications Union Recommendation 601-1 "Encoding Parameters of Digital Television"*. Excess 128 notation is assumed to be used for the Cr and Cb channels. The value of 128 identifies the 0 point within a range of 225 quantization levels for the Cr and Cb channels. The result is rounded to 8 bits -- values less than 0 are set to 0, and values greater than 255 are set to 255. Fields CSCE in Registers IPU1_MCR1 specify whether the Color Space Converter is enabled or bypassed for each field time.

3.3.2.4 LUT RAM

The LUT RAM is a programmable Look Up Table (LUT) comprised of three independent, 8-bit channels, each containing 256 8 bit read/write elements. Each LUT accepts input from one of the 8-bit output channels of the Input Format Converter.

The LUT RAM performs the following functions:

- gamma correction,

- RGB or YCbCr production from 8 bit pseudocolor data,
- point transforming (any input to output pixel mapping dependent on the input pixel value)

Fields LE in Registers IPU1_MCR1 specify whether the LUT RAM is enabled or bypassed for each field time.

NOTE: Although the LUT RAM can be enabled or bypassed independently each field time, only one lookup function is possible during both fields times. Therefore, the controlling software application must either perform identical operations during both field times, or bypass the LUT RAM during one field time.

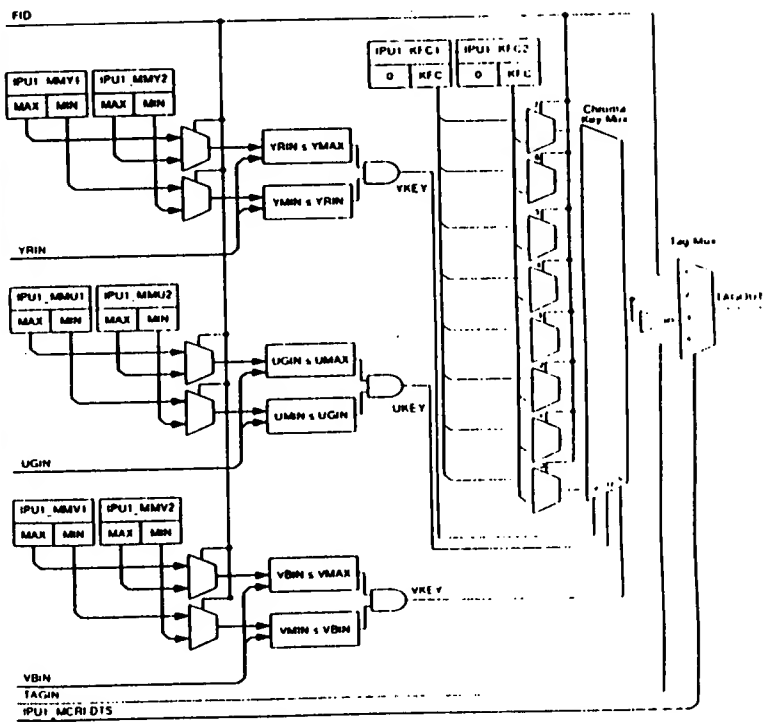


Figure 3-17. Input Tag Unit

3.3.2.5 X Prescaler

The X Prescaler is a 2:1 decimator; that is, it drops all even numbered pixels. Data along the Y axis remains unchanged. Fields PSE within Registers IPU1_MCRI specify whether the X Prescaler is enabled or bypassed.

3.3.2.6 Window Clipping and XY Scaler

The Window Clipping and XY Scaler, shown in Figure 3-18, has two functions:

- The IPU1 Window Clipping Unit clips the input stream into a rectangular region.
- The Y Scaler and X Scaler perform independent vertical and horizontal scaling.
  - The Y Scaler uses a nearest neighbor (decimation) algorithm to selectively drop full rows from the input stream. (A Special Y Scaling Path Mode using interpolation is described on page 57.)
  - The X Scaler uses linear interpolation for horizontal scaling.

Registers within the Window Clipping and XY Scaler define the clipping window coordinates and the X and Y scaling values for each field time.

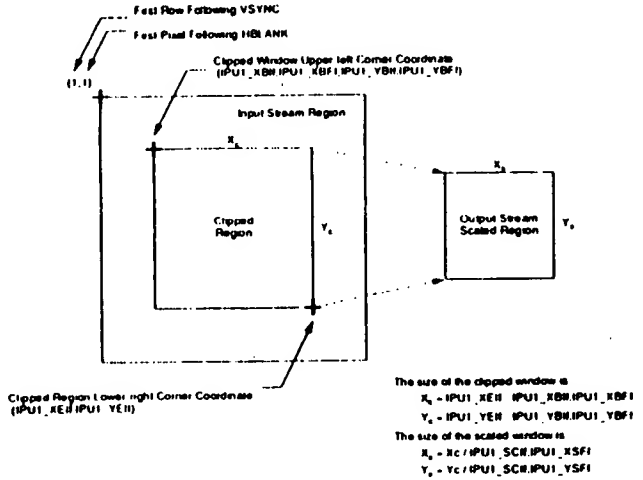


Figure 3-18. Window Clipping and XY Scaling Control Registers

IPU1 Window Clipping Unit

The Window Clipping Unit defines the clipping window — a rectangular area in the input video data stream. The clipping window can be a region of only a few pixels per side, up to the entire input stream, and is defined by the following registers:

- Registers IPU1_XBnI and IPU1_YBnI specify the upper left corner of the clipping window.
- Registers IPU1_XEnI and IPU1_YEnI specify the lower right corner of the clipping window.

NOTE: X and Y scaling logic processes only those pixels within the clipping window; it ignores all pixels outside the window and does not generate any output for them. The upper left coordinate of the clipping window can be a fractional value, indicating a starting column between two pixels, or a starting row between two rows.

Y Scaler

The Y Scaler uses a nearest neighbor (decimation) algorithm to scale an image vertically and maintains a row index generator and an 11-bit row counter. At the beginning of each field:

- the row index generator resets to the value programmed into Registers IPU1_YBnI, and
- the row counter resets to 1 for field 1, and to 2 for field 2 (interlaced data only).

The row counter determines if the current row lies within the clipped region. For each row input to the Y scaler, the row counter increments by 1 for progressive scan data, and increments by 2 for interlaced data. The current row is output when it lies within the clipped region and is within one row of the row index generator value. The row index generator value then increments by the Y shrink value programmed into Registers IPU1_YSnI. This procedure repeats until the current row reaches the boundary of the clipped region.

Registers IPU1_YSnI specify the vertical scaling factor as a 6.10 fixed point shrink value. The following equation specifies how the shrink value is used:

$$\text{output row count} = \frac{\text{input clipped row count}}{\text{IPU1\_YSnI}}$$

X Scaler

The X Scaler uses an interpolation circuit that maintains a pixel index generator and an 11-bit pixel counter. At the beginning of each row, the pixel index generator resets to the value programmed into Registers IPU1_XBnI, and the pixel counter resets to 1. The pixel counter determines if the current pixel lies within the clipped region, and it increments by 1 for each pixel processed by the X Scaler. When the current pixel lies within the clipped region and is within one pixel of the pixel index generator value, the interpolation circuit produces an output pixel. The pixel index generator value then increments by the X shrink value specified by Registers IPU1_XSnI. This procedure repeats until the current pixel lies outside the clipped region.

Registers IPU1_XSnI specify the horizontal scaling factor as a 6.10 fixed point shrink value. The following equation specifies how the shrink value is used:

$$\text{output pixel count} = \frac{\text{input clipped pixel count}}{\text{IPU1\_XSnI}}$$

NOTE: The Frame Buffer Data Bus transports data as pixel pairs. Therefore, the controlling software application must ensure that the Window Clipping Unit and the X Scaler produce an even number of pixels per row. FIFO G will not operate correctly when an odd number of pixels per row is produced.

Special Y Scaling Path Mode

The Y Scaler works with the ALU to implement a special two line vertical interpolation using an alternate stored in the frame buffer (in contrast to the decimation method). This mode is specified by field YSP in

Registers IPU1_MCRI, and field AOP in Registers ALU_MCRI. See also: ALU: Arithmetic and Logic Unit, page 63, Table 3-23, and Section 4.3.2.8 on page 109.

3.3.2.7 IPU1 Interrupt Request Unit

The IPU1 contains pixel, line, and field count registers that provide input stream based interrupt requests based on any combination of line and field counts. These registers are described in Table 3-17.

Table 3-17. IPU1 Interrupt Request Unit — Control Registers

Register	Field	Function
IPU1_PIX	—	**Pixel count Register.** This 11-bit upcounter is incremented as each pixel is input to the IPU1; it is automatically reset to 0 at the beginning of each line
IPU1_LIC	—	**Line count Register.** This 11-bit upcounter is incremented at the beginning of each line input to the IPU1; it is automatically reset to 0 at the beginning of each field. Its LSb specifies the field ID for interlaced sources: 0 = field 1, 1 = field 2.
IPU1_FLC	—	**Field count Register.** This 16-bit upcounter is incremented at the beginning of each field input to the IPU1. Unlike the pixel and line counters, the field counter can be reset under software control (see Register IPU1_FIR below).
IPU1_LIR	—	**Line Count Interrupt Request.** Specifies the 11-bit line count value at which an interrupt request should be generated.
IPU1_FIR	—	**Field Count Interrupt Request.** Specifies the 16-bit field count value at which an interrupt request should be generated. While bit 15 of this register = 0, Field Count Register IPU1_FLC is held at a count of 0. See Section 4.1.5 for more information on the interrupt request system of the CL-PX2070.

3.3.2.8 Output Format Converter Unit

The Output Format Converter Unit packs the 25 bit video stream used exclusively within the IPU1 into the pixel-pair format used by the internal Frame Buffer Data Bus and the Frame Buffer. It does not perform color space conversion. It supports the output formats shown in Table 3-18.

Table 3-18. Frame Buffer Data Formats

NOTE: These formats are shown for consecutive input pixels a d

Frame Buffer Bit	YCbCr 4:2:2 Non-tagged	4:2:2 Tagged	RGB 5:6:5 Non-tagged	5:5:5 Non-Tagged	5:5:5 Tagged	8:8:8 Non-Tagged	8:8:8 Tagged	3:3:2 16-bit	3:3:2 32-bit
FBD31	$Y7_b$	$Y7_b$	$R7_b$	—	T_b	...	T_a	—	$R7_a$
FBD30	$Y6_b$	$Y6_b$	$R6_b$	$R7_b$	$R7_a$	...	...	-	$R6_a$
FBD29	$Y5_b$	$Y5_b$	$R5_b$	$R6_b$	$R6_b$	...	...	-	$R5_a$
FBD28	$Y4_b$	$Y4_b$	$R4_b$	$R5_b$	$R5_b$	-	...	...	$G7_a$
FBD27	$Y3_b$	$Y3_b$	$R3_b$	$R4_b$	$R4_b$		...	...	$G6_a$
FBD26	$Y2_b$	$Y2_b$	$G7_b$	$R3_b$	$R3_b$	—	-	-	$G5_a$
FBD25	$Y1_b$	$Y1_b$	$G6_b$	$G7_b$	$G7_b$	...	-		$B7_a$
FBD24	$Y0_b$	$Y0_b$	$G5_b$	$G6_b$	$G6_b$	...	...	-	$B6_a$
FBD23	$V7_a$	$V7_a$	$G4_b$	$G5_b$	$G5_b$	$R7_a$	$R7_a$	...	$R7_a$
FBD22	$V6_a$	$V6_a$	$G3_b$	$G4_b$	$G4_b$	$R6_a$	$R6_a$	...	$R6_a$
FBD21	$V5_a$	$V5_a$	$G2_b$	$G3_b$	$G3_b$	$R5_a$	$R5_a$	...	$R5_a$
FBD20	$V4_a$	$V4_a$	$B7_b$	$B7_b$	$B7_b$	$R4_a$	$R4_a$	-	$G7_a$
FBD19	$V3_a$	$V3_a$	$B6_b$	$B6_b$	$B6_b$	$R3_a$	$R3_a$		$G6_a$
FBD18	$V2_a$	$V2_a$	$B5_b$	$B5_b$	$B5_b$	$R2_a$	$R2_a$	-	$G5_a$
FBD17	$V1_a$	$V1_a$	$B4_b$	$B4_b$	$B4_b$	$R1_a$	$R1_a$	-	$B7_a$
FBD16	$V0_a$	T_b	$B3_b$	$B3_b$	$B3_b$	$R0_a$	$R0_a$	-	$B6_a$
FBD15	$Y7_a$	$Y7_a$	$R7_a$	—	T_a	$G7_a$	$G7_a$	$R7_b$	$R7_b$
FBD14	$Y6_a$	$Y6_a$	$R6_a$	$R7_a$	$R7_a$	$G6_a$	$G6_a$	$R6_b$	$R6_b$
FBD13	$Y5_a$	$Y5_a$	$R5_a$	$R6_a$	$R6_a$	$G5_a$	$G5_a$	$R5_b$	$R5_b$
FBD12	$Y4_a$	$Y4_a$	$R4_a$	$R5_a$	$R5_a$	$G4_a$	$G4_a$	$G7_b$	$G7_b$
FBD11	$Y3_a$	$Y3_a$	$R3_a$	$R4_a$	$R4_a$	$G3_a$	$G3_a$	$G6_b$	$G6_b$
FBD10	$Y2_a$	$Y2_a$	$G7_a$	$R3_a$	$R3_a$	$G2_a$	$G2_a$	$G5_b$	$G5_b$
FBD9	$Y1_a$	$Y1_a$	$G6_a$	$G7_a$	$G7_a$	$G1_a$	$G1_a$	$B7_b$	$B7_b$
FBD8	$Y0_a$	$Y0_a$	$G5_a$	$G6_a$	$G6_a$	$G0_a$	$G0_a$	$B6_b$	$B6_b$
FBD7	$U7_a$	$U7_a$	$G4_a$	$G5_a$	$G5_a$	$B7_a$	$B7_a$	$R7_a$	$R7_a$
FBD6	$U6_a$	$U6_a$	$G3_a$	$G4_a$	$G4_a$	$B6_a$	$B6_a$	$R6_a$	$R6_a$
FBD5	$U5_a$	$U5_a$	$G2_a$	$G3_a$	$G3_a$	$B5_a$	$B5_a$	$R5_a$	$R5_a$
FBD4	$U4_a$	$U4_a$	$B7_a$	$B7_a$	$B7_a$	$B4_a$	$B4_a$	$G7_a$	$G7_a$
FBD3	$U3_a$	$U3_a$	$B6_a$	$B6_a$	$B6_a$	$B3_a$	$B3_a$	$G6_a$	$G6_a$
FBD2	$U2_a$	$U2_a$	$B5_a$	$B5_a$	$B5_a$	$B2_a$	$B2_a$	$G5_a$	$G5_a$
FBD1	$U1_a$	$U1_a$	$B4_a$	$B4_a$	$B4_a$	$B1_a$	$B1_a$	$B7_a$	$B7_a$
FBD0	$U0_a$	T_a	$B3_a$	$B3_a$	$B3_a$	$B0_a$	$B0_a$	$B6_a$	$B6_a$

NOTE: The controlling application software must track the format of the video stream being processed within the IPU1 and the Frame Buffer for both field times. For example, it would be invalid to specify an RGB input stream with an output YCbCr stream. The 25 bit RGB stream formed by the Input Format Converter must remain RGB data because the Output Format Converter Unit cannot perform the color space conversion necessary to produce the specified YCbCr format. However, a YCbCr input stream could be specified with an RGB output stream since the input YCbCr stream would be converted into the internal 25 bit YCbCr format, then to RGB using the Color Space Converter. This data is then packed into the specified RGB format for use by the internal Frame Buffer Data Bus and the external Frame Buffer.

3.3.3 IPU2: Input Processor Unit 2

The IPU2, shown in Figure 3-19, prepares an input video stream for ALU processing and/or storage in the Frame Buffer. The stream is output through FIFO F.

The IPU2 has two Master Control Registers (IPU2_MCR1 and IPU2_MCR2), allowing the IPU2 to perform different operations on two independent, field-synchronized, single field video streams during a common frame time. Field ID Signal FID, shown in Figure 3-19, determines the register set to be used. See also: Field Toggling and Field ID, page 42.

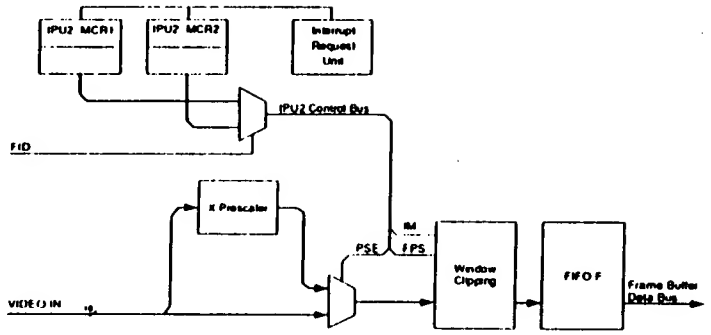


Figure 3-19. Input Processing Unit 2

The IPU2 contains three subunits, each of which is detailed in the following paragraphs:

- IPU2 X Prescaler
- IPU2 Window Clipping Unit
- IPU2 Interrupt Request Unit

3.3.3.1 IPU2 X Prescaler

The X Prescaler is a 2:1 decimator designed specifically for 4:2:2 YCbCr input streams. It drops every second luminance channel value, and every second chrominance channel pair values, as shown in Figure 3-20. Data along the Y axis of the input stream is unchanged. Fields PSE within Registers IPU2_MCR1 specify whether the X Prescaler is enabled or bypassed.

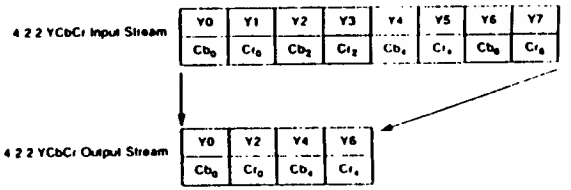


Figure 3-20. IPU2 2:1 Prescale Example

3.3.3.2 IPU2 Window Clipping Unit

The Window Clipping Unit, shown in Figure 3-21, defines the clipping window – a rectangular area of interest in the input video data stream. The clipping window can be a region of only a few pixels per side, up to the entire input stream, and is defined by the following registers:

- Registers IPU2_XBtl and IPU2_YBtl specify the upper left corner of the clipping window.
- Registers IPU2_XEtl and IPU2_YEtl specify the lower right corner of the clipping window.

NOTE: The Frame Buffer Data Bus transports data as pixel pairs. Therefore, the controlling application software must ensure that the Window Clipping Unit produces an even number of pixels per row. FIFO F will not operate correctly if an odd number of pixels per row is produced.

Table 3-19. IPU2 Window Clipping Unit — Control Registers

Register	Field	Function
IPU2_MCR1	IM	**Interlace Mode.** Specifies whether the input stream is interlaced or non-interlaced.
IPU2_MCR1	FPS	**Field Polarity Select.** Specifies the sync polarity of the input stream.

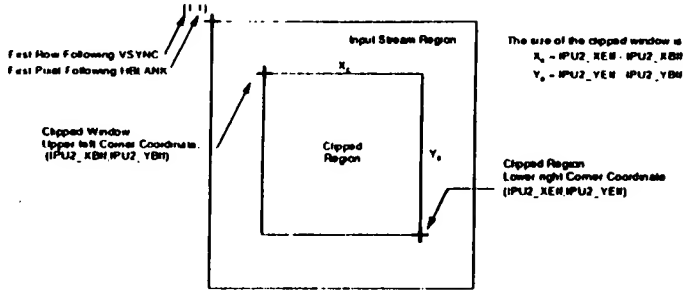


Figure 3-21. IPU2 Window Clipping Unit

3.3.3.3 IPU2 Interrupt Request Unit

The IPU2 contains Pixel, Line, and Field Count Registers, described in Table 3-20, that provide input stream based interrupt requests based on any combination of line and field counts.

Table 3-20. IPU2 Interrupt Request Unit — Control Registers

Register	Field	Function
IPU2_PIX	—	Pixel count Register. This 11 bit upcounter is incremented as each pixel is input to the IPU2. It is automatically reset to 0 at the beginning of each line.
IPU2_LIC	—	Line count Register. This 11 bit upcounter is incremented at the beginning of each line input to the IPU2. It is automatically reset to 0 at the beginning of each field. Its LSb specifies the field ID for interlaced sources: 0 = field 1, 1 = field 2.
IPU2_FLC	—	Field count Register. This 16 bit upcounter is incremented at the beginning of each field input to the IPU2. Unlike the pixel and line counters, the field counter can be reset under software control (see Register IPU1_FIR below).
IPU2_LIR	—	Line Count Interrupt Request. Specifies the 11-bit line count value at which an interrupt request should be generated.
IPU2_FIR	—	Field Count Interrupt Request. Specifies the 16 bit field count value at which an interrupt request should be generated. While bit 15 of this register = 0, Field Count Register IPU1_FLC is held at a count of 0. See Section 4.1.5 for more information on the Interrupt Request System of the CL-PX2070.

3.3.4 ALU: Arithmetic and Logic Unit

The ALU, shown in simplified form in Figure 3-22, is actually more than its name implies. It can operate on a pixel logically or arithmetically, or replace it or one of its component values with a constant. It can decode and/or encode pixels tags. A simplified block diagram is shown below.

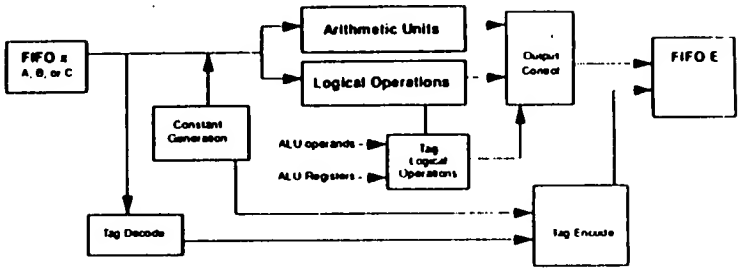


Figure 3-22. ALU Simplified Block Diagram

The ALU, shown in Figure 3-23, processes two simultaneous input video streams through FIFOs A and B, as well as the mask or mixing controls through FIFO C. Processed streams output through FIFO E.

The ALU accepts the following input streams and performs the corresponding function for each:

- tagged and non-tagged YCbCr — arithmetic, logical, and tagging operations;
- tagged and non-tagged RGB — logical and tagging operations.
- 8-bit pseudocolor input streams — logical and tagging operations.

Arithmetic and logical operations are mutually exclusive during a single field time.

Registers ALU_MCRI control stream format, operand source selection, tagging operation selection, and arithmetic or logical operation for both field times. Table 3-23 lists the arithmetic operations.

Like most of the other VPU subunits, the ALU has dual processors. Field ID Signal FID determines the register set to be used (refer to Section 3.2.2.2 on page 42).

The ALU has five primary functions, which are described in the following subsections:

- Operand Selection
- Data Tagging
- Logical Operations
- Arithmetic Operations
- Output Selection.

Section 3.3.4.6 describes the special Y Scaling Path. Refer to Figure 3-23 for all discussions of the ALU.

3.3.4.1 Operand Selection

The ALU contains three input FIFOs – A, B, and C. Data input to FIFO A sources Operand A (OpA), data input to FIFO B sources Operand B (OpB), and data input to FIFO C sources Operand C (OpC). With the exception of the special Y Scaling Path and bit per-pixel controls in OpC, each input FIFO and its operand selection circuit are identical.

YCbCr input streams are subdivided into separate 8-bit Y, Cb, and Cr component channels. RGB input streams are subdivided into separate 8-bit R, G, and B component channels.

Table 3-21. Operand Selection — Control Registers

Register	Field	Function
ALU_CAx	—	Constant A, Channels YUV. Specifies the 8-bit constant values to supply to each component channel and the tag bit
ALU_MCRI	OPAS OPBS OPCS	Operands ABC Source Select. Specifies whether the OpA multiplexers select the real time video stream or the contents of Registers ALU_CAx as the input for the logical and/or arithmetic sections. NOTE: Field OPAS controls four multiplexers simultaneously: the YR, CbG, and CrB component channels and the tag bit. Real-time stream data and constant data cannot be mixed in the same operand during the same field. However, for a given operand, real time stream data can be selected during one field 1, and constant data during the field 2

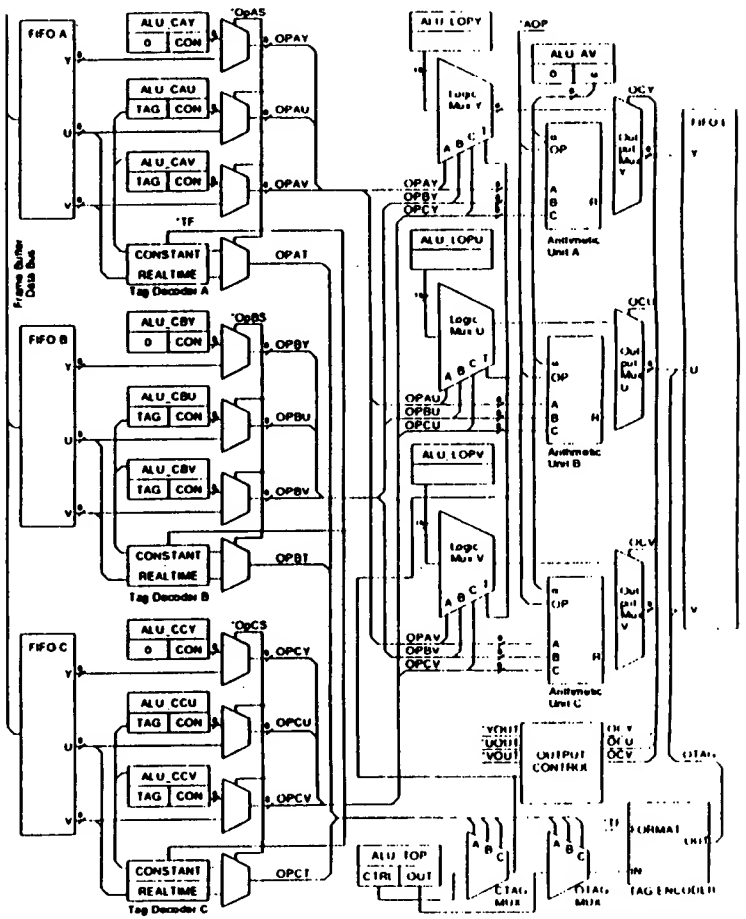


Figure 3-23. ALU: Arithmetic and Logic Unit

3.3.4.2 Data Tagging

Data tagging in the ALU performs three independent tasks:

- Logical operation,
- output multiplexer control, and
- output stream tag value.

The operand selection multiplexers select either the realtime tag or a constant tag as specified by the operand selection fields OPAS, OPBS, and OPCS (see Section 3.3.4.1). The control tag (CTAG) and the output tag (OTAG) are generated identically.

Table 3-22. Data Tagging — Control Registers

Register	Field	Function
ALU_MCRI	OPAS OPBS OPCS	**Operands ABC Source Select.** Specifies that the operand selection multiplexers select either the realtime tag or a constant tag (see Section 3.3.4.1).
ALU_MCRI	TF	**Tag Format.** Specifies the format of both the input and output streams

NOTE: Specifying "No Tag" ensures that no tag bit will be added to the output stream (see Section 4.3.5.1). However, a constant tag could be generated for one of the operands, which in turn could be used by the logical operations or output multiplexers. Similarly, one of the tagged data formats could be specified. The output tag multiplexer could be programmed to pass the tag unchanged, or override the input tag with a new value. In either case, the format of the stream cannot be changed. The controlling software application must ensure that the input tag, the generation of the internal CTAG and OTAG controls, and the output stream tagging are consistent with the desired operation and stream format.

Logical Operation Control

The tag bits from each operand are combined at the control tag multiplexer. This combination specifies the input bit to be selected from field CTC of Register ALU_TOP to generate CTAG. CTAG is one of four control signals provided to the logical operation multiplexers, and is also used by the output control section, as described in Section 3.3.4.5. Since each operand contributes a single, realtime control bit to the CTAG multiplexer, logical operations and output selection can be controlled on a pixel-by-pixel basis.

Output Multiplexer Control

In the same way, the tag bits from each operand specify the input bit to be selected by the output tag multiplexer from field OTC of Register ALU_TOP to generate OTAG. OTAG is the output tag value that FIFO E adds to the output stream. Since each operand contributes a single, realtime control bit to the OTAG multiplexer, the output tag can be controlled on a pixel by pixel basis.

Output Stream Tag Value

The value of the output tag is encoded under control of the TF field in ALU_MCR, then passed to the output FIFO.

3.3.4.3 Logical Operations

The ALU performs logical operations using eight parallel 16:1 multiplexers, each providing one bit to the 8-bit output stream. Register ALU_LOPY specifies the 16 bit input to all eight multiplexers.

The CTAG control and eight bits from each channel of each operand provide a 4 bit input selection control to the multiplexer. Each 16:1 multiplexer uses a different bit from each of the channel streams - the first uses bit 0 from each stream, the second uses bit 1, etc. All eight multiplexers share the CTAG value. Different operations can be programmed for each channel of the same input stream.

3.3.4.4 Arithmetic Operations

The arithmetic sections of the ALU only process YCbCr input streams. They do not support RGB streams. The arithmetic unit performs eight operations, as shown in Table 3-23.

Table 3-23. Arithmetic Operations

NOTE: U = unsigned 8 bit (Uses excess 128 notation where appropriate. See also 3.3.2.3, page 54.)
S = signed 8-bit

OpA	OpB	OpC	E	Formula	Function
U	U	—	U	E = (A*α) + (B*(1-α))	Alpha mix using ALU_AV
U	U	U	U	E = (A*C) + (B*(1-C))	Alpha mix using C
U	U	—	U	E = A + B	Add A and B
U	U	—	U	E = A - B	Subtract B from A
U	U	—	S	E = (A - B) / 2	Difference A to B
U	S	—	U	E = A + (2*B)	Reconstruct from A and B
U	S	—	U	E = A + ((2*B) / 4)	Four frame interpolate from A and B
U	U	—	U	E = (A*n[a]) + (B*(1-n))	Special ALU Y Scaling Path

a n = fractional pixel value from IPU2 scaler

Table 3-24. Arithmetic Operations — Control Registers

Register	Field	Function
ALU_MCRI	AOP	**Arithmetic Operation Select.** Specify the arithmetic operation to perform for each field time
ALU_AV	—	**Alpha value.** Specifies the alpha mix value when performing a constant alpha mix

3.3.4.5 Output Selection

The output multiplexers select between the output of the logical operation multiplexers and the arithmetic unit CTAG and fields YOUT, UOUT, and VOUT of Registers ALU_MCRI specify the output selection of each output multiplexer. Since CTAG is generated by the realtime input stream, output selection can be made pixel by pixel.

3.3.4.6 Special α-Mixed Y Scaling Mode

The Y scaler, in combination with the ALU, provides a special mode of operation in which a 2-line interpolation scales in the Y direction using a table of α values (as opposed to the decimation method). Fields YSP in Registers IPU1_MCRI and field AOP in Registers ALU_MCRI specify this mode (see Section 3.3.2.6 on page 56).

3.3.5 OPU: Output Processor Unit

The OPU, shown in Figure 3-24, converts the stream data written to FIFO D from the format used in the Frame Buffer to an output stream format. The OPU contains three subunits, each of which is detailed in the following paragraphs:

- Output Format Converter
- 2:1 X Zoom Unit
- OPU Window Clipping Unit.

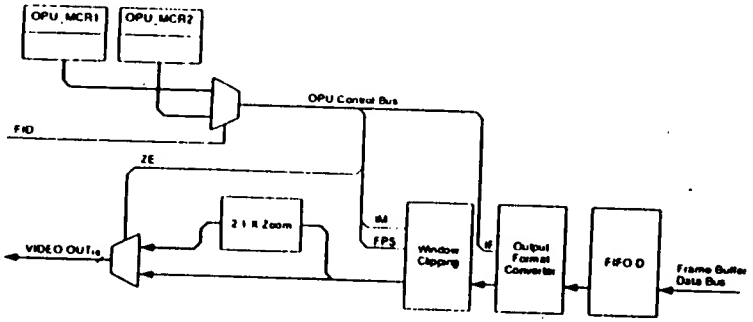


Figure 3-24. OPU: Output Processor Unit

The OPU has two Master Control Registers (OPU_MCR1 and OPU_MCR2) — one for each field time — allowing the OPU to perform different operations on two independent, single-field video streams during a common frame time. Field ID Signal FID determines the register set to be used. See also: Field Toggling and Field ID, page 42).

NOTE: The Frame Buffer Data Bus transports data as pixel pairs. Therefore, the controlling application software must ensure that FIFO D receives an even number of pixels per row. FIFO D will not operate correctly if it receives an odd number of pixels per row.

3.3.5.1 Output Format Converter

The Output Format Converter unpacks the pixel pair stream data written to FIFO D into one of five formats for transport to the VRU. The OPU supports two YCbCr and three RGB formats.

The OPU supports two YCbCr and three RGB formats (refer to Table 3-14, Table 3-15, Table 3-16, and Table 3-18):

- YCbCr 4:2:2 non-tagged
- YCbCr 4:2:2 tagged
- RGB 5:6:5 non-tagged
- RGB 5:5:5 tagged
- RGB 3:3:2 non-tagged.

NOTE: The OPU does not convert between YCbCr and RGB formats. The controlling software application must track the format of the video stream transported from the Frame Buffer to the OPU for both field times. For example, it would be invalid to specify an RGB output stream if the Frame Buffer is actually supplying a YCbCr stream.

3.3.5.2 2:1 X Zoom Unit

The 2:1 X Zoom Unit performs a 2-to-1 zoom along the X axis of the output stream. That is, it outputs exactly twice the number of pixels input. A linear interpolation unit generates a new pixel with a value average that of the pixels on either side.

The 2:1 X Zoom Unit does not support RGB 3:3:2 non-tagged output streams.

3.3.5.3 OPU Window Clipping Unit

The Window Clipping Unit defines the clipping window — a rectangular area of interest in the stream transported from the Frame Buffer Data Bus. The clipping window can be a region of only a few pixels per side, up to the entire input stream, and is defined by the following registers:

- Registers OPU_XBII and OPU_YBII specify the upper left corner of the clipping window.
- Registers OPU_XBII and OPU_YEII specify the lower-right corner of the clipping window.

Table 3-25. OPU Window Clipping Unit — Control Registers

Register	Field	Function
OPU_MCRI	IM	**Interlace Mode.** Specifies whether the input stream is interlaced or non-interlaced.
OPU_MCRI	FPS	**Field Polarity Select.** Specifies the sync polarity of the input stream.

3.4 RFU: Reference Frame Unit

The RFU, shown in Figure 3-25, creates and manages multiple reference frames, and provides simultaneous access to eight object buffers and four display windows.

The RFU contains three subunits, each of which is detailed in the following sections:

- OBU: Object Buffer Unit
- DWU: Display Window Unit
- MMU: Memory Management Unit.

The OBU and DWU Registers control the operation of the RFU.

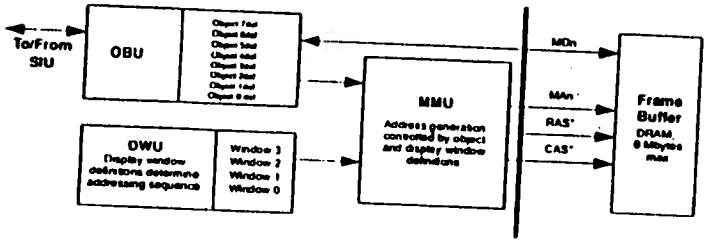


Figure 3-25. The Reference Frame Unit

Reference frames are rectangular, two dimensional regions of the Frame Buffer that are allocated and deallocated as necessary by the controlling software application; they can be any size, order, or location, and can be contiguous or separated.

The name *reference frame* comes from the manner by which the RFU manages the frame buffer. Rather than re-arranging graphics objects by recopying bitmaps, the CL-PX2070 moves the frame of reference around the data that represents the object. A number of virtual frame buffers can exist within the physical frame buffer.

NOTE: The number of virtual reference frames which can be allocated is limited only by the total amount of memory available in the Frame Buffer. However, there can be no more than eight physical, simultaneous reference frames (since the CL-PX2070 contains only eight object buffer register sets).

The RFU accesses the Frame Buffer using linear rather than rectangular addresses, as shown in Figure 3-26. Although all storage elements are 16 bits wide, the Frame Buffer is addressable only on 32-bit, or pixel pair, boundaries; therefore, the LSb of the address is always treated as 0h, regardless of the value written by the controlling software application. The bit assignments used by the Frame Buffer Data Bus FBD[31:0] are listed in Table 3-18.

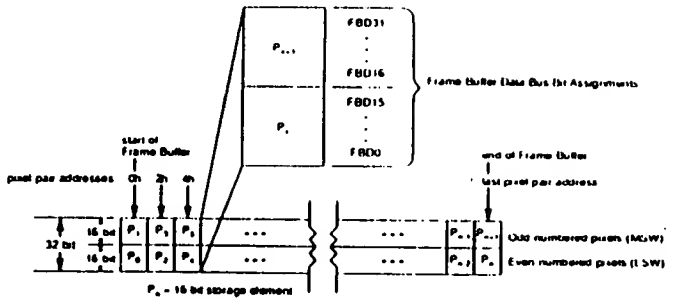


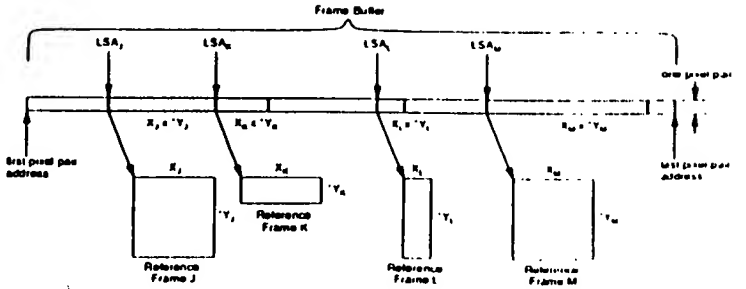
Figure 3-26. Frame Buffer Addressing (32-bit)

The Linear Start Address (LSA) represents the upper-left corner (coordinate (0,0)) of the reference frame. It specifies the start of the reference frame relative to the start of the Frame Buffer (physical address 00000h).

NOTE: The CL-PX2070 does not specify a height parameter when defining a reference frame. The controlling software application must ensure that the object buffers and display windows are located within the intended boundaries.

The linear addressing architecture of the RFU allows reference frames to be allocated from contiguous, one-dimensional strings of memory, rather than inefficient rectangular areas typical in simpler architectures. A reference frame is specified by two values, as shown in Figure 3-27:

- the LSA, and
- the width in 16-bit pixels.



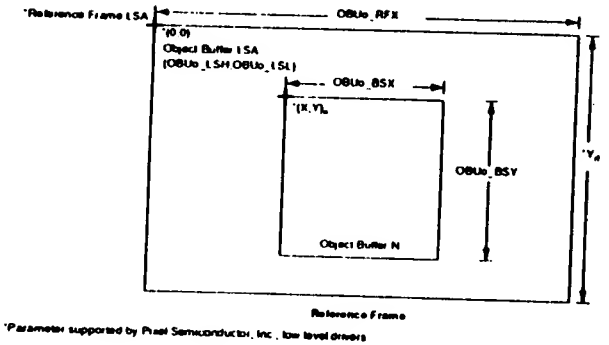
*Dimension must be implied by the controlling software application; it is not programmed into the CL-PX2070.

Figure 3-27. Reference Frame Allocation

3.4.1 OBU: Object Buffer Unit

The OBU creates and manages up to eight physical, simultaneous object buffers, each of which can be programmed (via its *linear start address*, or *LSA*) to be located anywhere in the frame buffer memory.

The object buffer, shown in Figure 3-28, is a rectangular, two-dimensional storage region allocated within a reference frame. *The object buffer is the only means by which data can be stored to or retrieved from the Frame Buffer.*



*Parameter supported by Pixel Semiconductor, Inc.; low level drivers

Figure 3-28. Object Buffer

The OBU allows each object buffer to be locked to either video source, or to be programmed to operate independently. Object buffers also can be placed anywhere within the linearly-addressable Frame Buffer. One pair of registers for each object buffer completely specify an object buffer and locate it within a reference frame, as shown in Table 3-26.

Table 3-26. Object Buffers — Control Registers

Register	Field	Function
OBUo_LSb	—	**Display Window Linear Start Address.** Specifies the location of the object buffer. This physical location represents a corner of the rectangular region relative to the start of the Frame Buffer (physical location 00000h), *not relative to the reference frame.*
OBUo_MCR	XBDC, YBDC	**XY BLT Direction Control.** Determine which corner of the object buffer is specified.
OBUo_RFX	—	**Object Buffer Reference Frame X Size.** Specifies the X dimension (pitch) of the reference frame in 16-bit pixels. OBUo_RFX is the only OBU Register that has any direct, hardware control of the reference frame.
OBUo_BSa	—	**Object Buffer Size.** Specifies the X and Y dimensions of the object buffer in 16 bit pixels.
OBUo_RFX	RFX	the X dimension of the reference frame, within which the object buffer is relatively located (the Y dimension is implied by number of lines).
OBUo_BSX OBUo_BSY	BSX BSY	the X and Y size of the object;
OBUo_LSH OBUo_LSL	RSVD LSL	the starting pixel of the object buffer.
OBUo_DEC	DM7-DM0	output decimation — small preview windows which can be displayed at low band width.
OBUo_MCR	OPM	operating mode;
OBUo_MCR	XBDC YBDC	X and Y BLT directions;
OBUo_MCR	FA	FIFO association.
OBUo_MCR	LME CME	chrominance and luminance channel masking

An object resize operation illustrates the advantages of this arrangement - - the processor must only write to three registers to complete the resizing. "Tearing" is eliminated by only "moving" during the Vsync time.

Table 3-28. DWU: Display Window Unit — Control Registers *(cont.)*

Register	Field	Function
DWUd_DSY	—	Display Window Display Y Start. Specifies the number of rows between the top row of the CRT display and the top row of the display window
DWU_HCR	—	Display Window Horizontal Control Register. Specifies the total number of active pixels per row expected by the current sync parameters of the output CRT display device. (The number of rows to output is not required.)
DWUd_DZF	YZOOM, XZOOM	Functional only when used with CL-PX2080. Specifies zoom factor. The image is scaled according to the following formula: $\text{Scaling} = \frac{256}{\text{ZOOM FACTOR}}$

Operation with and without the CL-PX2080 MediaDAC™

The CL-PX2080 MediaDAC is a companion device for the CL-PX2070 that allows overlapping (occluded) display windows, as specified by field OCC in Register DWU_MCR.

- When the CL-PX2070 is used with the CL-PX2080, the system supports up to four occluded display windows.
- When the CL-PX2070 is used without the CL-PX2080, the display windows cannot overlap. In this case, the controlling software application *must* ensure that:
  - the display windows do not overlap;
  - adjacent display windows are separated by the minimum distance specified by Register DWU_HCR;
  - rows within a display window do not cross physical memory row boundaries.

NOTE: The value written into Register DWU_HCR depends upon the dotclock of the CRT display system. For more information, see 4.4.3.2, page 147. Use the following equation to determine the minimum possible value:

$$\text{MWS} = \frac{1\mu S}{\text{GPCLK period}}$$

3.4.4 MMU: Memory Management Unit

The MMU provides DRAM/VRAM support and translates the parameters from the rest of the system into physical memory addresses using Register MMU_MCR, as shown in Table 3-29. Frame buffer size can be up to 8 megabytes.

Table 3-29. MMU: Memory Management Unit — Control Registers

Register	Field	Function
MMU_MCR	FBC	Frame Buffer Configuration. Specifies the memory device, ensuring that the Frame Buffer is addressed correctly.
MMU_MCR	FBD	Frame Buffer Depth. Specifies the width of the Frame Buffer to be 16 or 32 bits wide. As shown in Figure 3-31, a 16-bit Frame Buffer is addressed identically to the 32-bit Frame Buffer, except that only the least significant 16-bit pixels can be accessed (the most significant 16-bit pixels do not exist). Note the following when using 16-bit mode: • 8-bit pseudocolor stream data is the input format normally used with 16-bit mode, as shown in Table 3-18. This 16-bit mode is the only mode in which the IPU1 output formatter fills only the lower 16 bits of the 32-bit Frame Buffer Data Bus. • 16-bit input streams can be used, but the input stream device must pack 16-bit pixels in the 32-bit format. • A 16-bit output stream can be used if the output stream device unpacks the 16-bit data from the 32-bit format of the OPU.

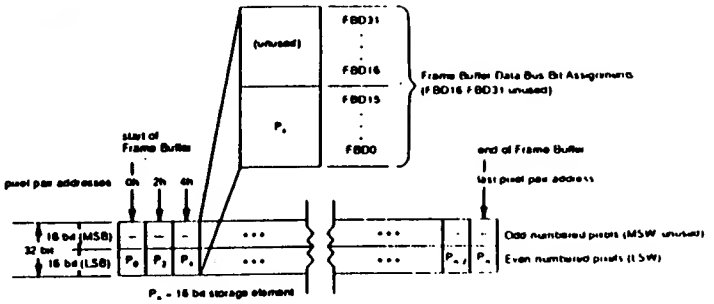


Figure 3-31. Frame Buffer Addressing (16-Bit)

3.4.4.1 Frame Buffer Architecture

The frame buffer is a DRAM/VRAM array with a 32 bit data bus (FBD[31:0]). Two RAS* signals are provided to select between two 32 bit banks. Four CAS* signals are provided, and are typically used for byte selection. The memory device size is chosen from the options in field FBC of the MMU_MCR register, described in Section 4.4.2.1 on page 145. Figure 3-32 shows a typical frame buffer implementation.

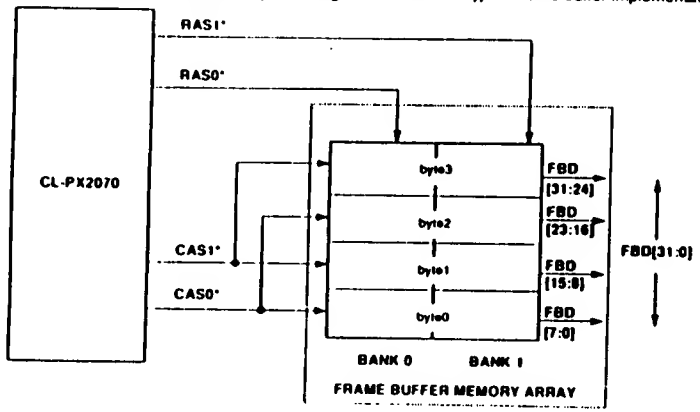


Figure 3-32. Typical Frame Buffer Implementation

4. DETAILED REGISTER DESCRIPTONS

This section lists and defines the CL-PX2070 registers. The registers are organized according to CL-PX2070 subsection.

NOTE: Register names containing lower-case variables represent groups of registers with similar functions. For example, VIU_DPC# represents both Datapath Control registers -- VIU_DPC1 (Datapath Control Field 1) and VIU_DPC2 (Datapath Control Field 2). Table 4-1 lists and defines all variables used in this manner.

In order to maintain compatibility with future Pixel Semiconductor products, all reserved bits in all registers must be written as zero.

Table 4-1. Variables Used in Register Names

Variable	Replaces	Variable	Replaces
a (axis)	X, Y	n (number)	F (Fraction) or I (Integer)
b (byte)	L (Low) or H (High)	o (object buffer #)	0-7
c (color space)	Y, U, V or R, G, B	p (port)	1-2
d (display window #)	0-3	s (SIM)	0-31
f (field)	1-2	x (channel)	Y, U, V

4.1 HIU: Host Interface Unit — Registers

Table 4-2. HIU Register Address Map

Register	Pri. Map	Sec. Map	Definition	Used by Registers		Ref. Section
HIU_0	27C0	0290	Register I/O Address 0	HIU_CSU	Configuration Setup	4.1.1, page 82
				HIU_DBG	Debug Control	4.1.2, page 83
				HIU_DRD	Debug Read	4.1.3, page 84
HIU_1	27C2	0292	Register I/O Address 1	HIU_OCS	Operation Control/Status	4.1.4, page 85
				HIU_IRQ	Interrupt Request	4.1.5, page 86
HIU_2	27C4	0294	Register I/O Address 2	HIU_RIN	Register Index	4.1.6, page 87
HIU_3	27C6	0296	Register I/O Address 3	HIU_RDT	Register Data Port	4.1.7, page 88
HIU_4	27C8	0298	Register I/O Address 4	HIU_MDT	Memory Data Port	4.1.8, page 88

Table 4-3. HIU Registers Accessed by the Register Data Port

Register	Index	Definition	Ref. Section
HIU_IMD	0000	Indexed Memory Data (Local Hardware Interface Mode)	4.1.9, page 88
HIU_ISU	0001	Interrupt Setup	4.1.10, page 89

4.1.1 HIU_CSU: Configuration Setup (Read Only)

I/O Address 27C0 (Primary Map)
0290 (Secondary Map)

See also. Section 3.1.1 on page 27

Register HIU_CSU stores hardware configuration data for the CL-PX2070. An external configuration register must provide configuration data to the LSB of HIU_CSU during the reset interval. HIU_CSU is shadowed by registers HIU_DBG and HIU_DRD.

RSVD2				VER				RSVD		HSB			RSVD	FBT	PAS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:12	R	0000	RSVD	Reserved (read as 0)
11:8	R	0000	VER	Video Processor Device Version 0000 CL-PX2070
7:6	R	000	RSVD	Reserved (read as 0 in ISA and MCA modes, read as 1 in local hardware interface mode)
5:3	R	111	HSB	Host System Bus. Specifies the type of host system connected to the CL-PX2070 000 ISA bus definition 100 Aux ISA 001 MCA bus definition 101 Aux MCA 010 Reserved 011, 111 Local hardware interface definition 1xx All other configurations reserved.
2	R	1	RSVD	Reserved (read as 1)
1	R	1	FBT	Frame Buffer Jumper State. 0 DRAM 1 VRAM
0	R	0	PAS	Port Address Select. Specifies the I/O address map that the host system should use when accessing the CL-PX2070. 0 Primary port map select 1 Secondary port map select

4.1.2 HIU_DBG: Debug Control (Write Only)

I/O Address 27C0 (Primary Map)
0290 (Secondary Map)

Register HIU_DBG controls the diagnostic mode of the CL-PX2070. Field MDE of register HIU_OCS must be set to 1 before write access to this register is enabled. HIU_DBG is shadowed by register HIU_DRD. Field DRE must be set to 1 before read access to register HIU_DRD is enabled.

RSVD						DRE	ORS		SSE	LE	SIMBP				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:10	R/W	0h	RSVD	Reserved (read as 0)
9	W	0	DRE	Debug Read Enable. Controls access to shadow register HIU_DRD 0 Disable debug read 1 Enable debug read
8:7	W	00	ORS	Operation Restart Select. Specifies the instruction index at which the SIU should restart 00 Restart from current index 01 Restart from SI1 10 Restart from SI2 11 Reserved
6	W	0	SSE	Single Step Enable. Controls the operation of the single step mode 0 Normal operation 1 Single step operation (auto reset)
5	W	0	EE	Execution Enable. Controls the operation of the SIU in debug mode 0 Halt CL-PX2070 1 Execute instruction (auto reset on breakpoint or single step)
4:0	W	0h	SIMBP	Sequence Instruction Memory Breakpoint. Specifies the instruction index at which SIU execution will halt during debug mode (0-1Fh)

4.1.3 HIU_DRD: Debug Read (Read Only)

I/O Address 27C0 (Primary Map)
0290 (Secondary Map)

See also. HIU_DBG Debug Control (Write Only), p. 83
HIU_OCS Operation Control/Status (Read/Write), p. 85
SIU_MCR Master Control, p. 124
SIUs_SIM Sequencer Instruction Memory, p. 127

Register HIU_DRD accesses diagnostic information provided by the global Error Detection Trap, the current object buffer counters, and the SIU current index. HIU_DRD is a shadow register to HIU_CSU. Field MDE of register HIU_OCS and field DRE of register HIU_DBG must be set to 1 before read access to this register is enabled.

EDT	XC					YC					SIMIN				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R	0	EDT	Error Detection Trap. This field is the logical OR of all FIFO overflow and underflow flags, and the watchdog timeout. 0 No error 1 Error detected
14 10	R	0h	XC	Upper 5 bits of X Counter (Single Step Mode) (0-1Fh)
9 5	R	0h	YC	Upper 5 bits of Y Counter (Single Step Mode) (0-1Fh)
4 0	R	0h	SIMIN	Sequence Instruction Memory Current Index (0-1Fh)

4.1.4 HIU_OCS: Operation Control/Status (Read/Write)

I/O Address 27C2h(Primary Map)
0292 (Secondary Map)

Register HIU_OCS controls the operating mode of the CL-PX2070 and provides status indicators. HIU_OCS is shadowed during read cycles by register HIU_IRQ (see field SRC below).

RSVD	FFH	FDH	DMAW	SRC	MDE	DPC	MPC	PMC	DMD	DME	SR	IEM			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R	0	RSVD	Reserved (read as 0)
14	R	0	FFH	FIFO F half full when read as 1
13	R	0	FDH	FIFO D half full when read as 1
12	R	0	DMAW	indicates DMA wait state when read as 1
11	R/W	0	SRC	Status Read Select. Specifies register to access during a read cycle 0 Read status from register HIU_OCS 1 Read status from shadow register HIU_IRQ
10	R/W	0	MDE	Master Debug Enable. Controls access to the debug support registers 0 Disable debug operation 1 Enable debug operation, enables access to registers HIU_DBG and HIU_DRD
9	R/W	0	DPC	Display Window Posting Operation Control (auto reset). Specifies the register posting mode of the DWU 0 Disable posting 1 Enable posting (auto reset on post)
8	R/W	0	MPC	Master Posting Control (auto reset). Enables or disables all register posting logic of the CL-PX2070 0 Disable posting 1 Enable posting (auto reset on post)
7	R/W	0	PMC	Posting Mode Control. Specifies normal register posting or forces an immediate register posting operation 0 Normal posting operation 1 Immediate post all registers (auto reset on post)
6	R/W	0	DMD	DMA Direction 0 DMA input to CL-PX2070 1 DMA output from CL-PX2070
5	R/W	0	DME	DMA Enable 0 Disable DMA transfers 1 Enable DMA transfers

Bit #	Access	Reset	Description (cont.)	
4	R/W	0	SFI	SFI Soft Reset (auto reset) Causes a soft reset to be performed on all internal units All registers are reset to 0, all FIFOs are cleared, and all counters are set to 0 Output signals are not placed in tristate 0 No reset performed 1 Perform soft reset (auto reset)
3 0	R/W	0000	IEM	IEM Interrupt Enable Mask This field enables or disables interrupt requests from the four major interrupt sources When more than one interrupt source is enabled, the requests are ORed-- any source can assert IRQ See Section 4 1 10 on page 89 for additional information on the interrupt system. 0001 Enable counter to generate signal IRQ 0010 Enable watchdog to generate signal IRQ 0100 Enable object buffer termination to generate signal IRQ 1000 Enable FIFO overflow/underflow to generate signal IRQ

4.1.5 HIU_IRQ: Interrupt Request (Read Only)

I/O Address 27C2 (Primary Map)
0292 (Secondary Map)

See also HIU_OCS Operation Control/Status (Read/Write), p 85
HIU_ISU Interrupt Setup, p 89

Register HIU_IRQ accesses all interrupt requests generated by the IPU1, the IPU2, the OBU, the Watchdog Timer, and the FIFO overflow and underflow flags An interrupt service routine typically uses HIU_IRQ to determine the interrupt request source(s) HIU_IRQ shadows register HIU_OCS. Field SRC of register HIU_OCS must be set to 1 before access to this register is enabled. An interrupt request appears as a 1, and inactive interrupt sources remain at 0.

RSVD										OBT	IP2C	IP1C	FUN	FOV	WDT
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 6	R	0h	RSVD	Reserved (read as 0)
5	R	0	OBT	Object Buffer Termination (auto reset on read) Indicates that an object buffer termination condition occurred in the OBU
4	R	0	IP2C	IPU2 Counter (auto reset on read) Indicates that a line, field, or vertical sync pulse interrupt request occurred in the IPU2.
3	R	0	IP1C	IPU1 Counter (auto reset on read) Indicates that a line, field, or vertical sync pulse interrupt request occurred in the IPU1
2	R	0	FUN	FIFO Underflow (auto reset on read) Indicates that an underflow condition occurred in a FIFO (SIU_FCS FIFO Control/Status, p 124)

Bit #	Access	Reset	Description (cont.)	
1	R	0	FOV	FIFO Overflow (auto reset on read) Indicates that an overflow condition occurred in a FIFO (SIU_FCS FIFO Control/Status, p 124)
0	R	0	WDT	Watchdog Timer to generate signal IRQ (auto reset on read) Indicates that a timeout condition occurred in the Watchdog Timer (VIU_WDT Watchdog Timer, p 94)

4.1.6 HIU_RIN: Register Index (Read/Write)

I/O Address 27C4 (Primary Map)
0294 (Secondary Map)

See also: HIU_IMD: Indexed Memory Data (Local Hardware Interface Mode), p 88

Register HIU_RIN specifies the index value of the next register to be accessed An optional control automatically increments the index address on consecutive access (read or write) cycles

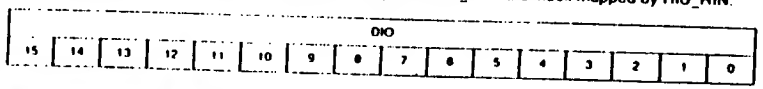
AIC	RIN													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	0h	AIC	Automatic Increment Control Controls the automatic increment feature of the index address 0 Disable automatic increment 1 Enable automatic increment
14 0	R/W	0h	RIN	Register Index (0-7FFFh)

4.1.7 HIU_RDT: Register Data Port

I/O Address 27C6 (Primary Map)
0296 (Secondary Map)

HIU_RDT is the register data port. All registers mapped to HIU_RDT are index mapped by HIU_RIN.

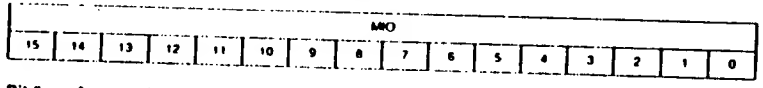


Bit #	Access	Reset	Description	
15:0	R/W	0h	DIO	Register Data I/O

4.1.8 HIU_MDT: Memory Data Port (Read/Write)

I/O Address 27C8 (Primary Map)
0298 (Secondary Map)

I/O port HIU_MDT accesses the Frame Buffer. To maintain data integrity when reading or writing to this port, first check the status of the appropriate FIFO.

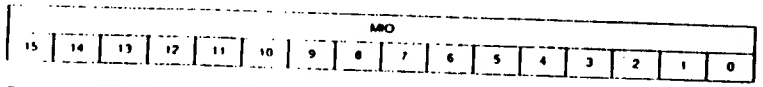


Bit #	Access	Reset	Description	
15:0	R/W	0h	MIO	Memory Data I/O

4.1.9 HIU_IMD: Indexed Memory Data (Local Hardware Interface Mode)

I/O Address HIU_RDT
Index 0000

Register HIU_IMD may be used to accesses the Frame Buffer when the CL-PX2070 is operating in local hardware interface mode. The CL-PX2070 accesses the Frame Buffer through register data port HIU_RDT when register HIU_IMD is specified.



Bit #	Access	Reset	Description	
15:0	R/W	0h	MIO	Memory Data I/O

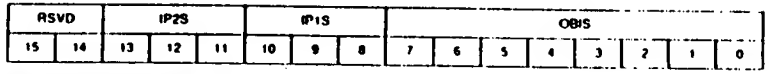
4.1.10 HIU_ISU: Interrupt Setup

I/O Address HIU_RDT
Index 0001

Register HIU_ISU specifies the interrupt modes for the IPU1, IPU2, and the OBU. Any interrupt requests generated in the IPU1, IPU2, and OBU must also be enabled through field IEM of register HIU_OCS.

IPU interrupts are combined with an AND function. If more than one interrupt source is enabled within an IPnS field, all sources must be active before an interrupt request is posted.

The interrupt sources in the OBIS field use an OR function. If more than one interrupt source is selected, any one active source can trigger an interrupt.



Bit #	Access	Reset		
15:14	R/W	00	RSVD	Reserved (read as 0)
13:11	R/W	000	IP2S	IPU2 Interrupt Select. Specifies the IPU2 line count, field count, and input vertical sync pulse combination required to generate an interrupt request 001 Interrupt on line count 010 Interrupt on field count 100 Interrupt on VSync
10:8	R/W	000	IP1S	IPU1 Interrupt Select. Specifies the IPU1 line count, field count, and input vertical sync pulse combination required to generate an interrupt request 001 Interrupt on line count 010 Interrupt on field count 100 Interrupt on VSync
7:0	R/W	0h	OBIS	Object Buffer Termination Interrupt Request. Specifies the OBU object buffer termination conditions combination required to generate an interrupt request signal IRQ 01h Object buffer 0 termination 02h Object buffer 1 termination 04h Object buffer 2 termination 08h Object buffer 3 termination 10h Object buffer 4 termination 20h Object buffer 5 termination 40h Object buffer 6 termination 80h Object buffer 7 termination

4.2 VBU: Video Bus Unit — Registers

Table 4-4. VBU Registers Accessed by the Register Data Port

Register	Index	Definition	Ref. Section
VIU: Video Interface Unit			4.2.1, page 91
VIU_MCR1	1000	Master Control V1	4.2.1.1, page 91
VIU_MCR2	1001	Master Control V2	4.2.1.1, page 91
VIU_DPC1	1002	Datapath Control Field 1	4.2.1.2, page 92
VIU_DPC2	1003	Datapath Control Field 2	4.2.1.2, page 92
VIU_WDT	1004	Watchdog Timer	4.2.1.3, page 94
VSU: Video Sync Unit			4.2.2, page 95
VSU_HSW	1100	Horizontal Sync Width	4.2.2.1, page 96
VSU_HAD	1101	Horizontal Active Delay	4.2.2.2, page 96
VSU_HAP	1102	Horizontal Active Pixels	4.2.2.3, page 97
VSU_HP	1103	Horizontal Period	4.2.2.4, page 97
VSU_VSW	1104	Vertical Sync Width	4.2.2.5, page 98
VSU_VAD	1105	Vertical Active Delay	4.2.2.6, page 98
VSU_VAP	1106	Vertical Active Pixels	4.2.2.7, page 99
VSU_VP	1107	Vertical Period	4.2.2.8, page 99

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4.2.1 VIU: Video Interface Unit

4.2.1.1 VIU_MCRp: Master Control

I/O Address HIU_RDT
Index 1000 (VIU_MCR1 Master Control V1)
1001 (VIU_MCR2 Master Control V2)

Registers VIU_MCR1 and VIU_MCR2 specify the functional and I/O characteristics of Video Port Interfaces 1 and 2.

STM	OFP	OSS		OVSP	OHSP	OBP	OBT	IFP	ISS	IVSP	IHSP	IBP	IBT	KM	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Res	Description
15	R/W	0	STM Stall Mode 0 stall mode disabled 1 stall mode enabled
14	R/W	0	OFP Output Video Field Polarity 0 normal polarity 1 inverted polarity
13 12	R/W	00	OSS Output Video Sync Source 00 Vsync, Hsync, and blank input to CL-PX2070 01 Vsync, Hsync input to CL-PX2070, blank output from OP 10 Vsync, Hsync, and blank output from VSU 11 Blank output from OPU
11	R/W	0	OVSP Output Video Vertical Sync Polarity. Specifies polarity of vertical sync signals V1VS (VIU_MCR1) and V2VS (VIU_MCR2) when signals are used as output 0 active low 1 active high
10	R/W	0	OHSP Output Video Horizontal Sync Polarity. Specifies polarity of horizontal sync signals V1HS (VIU_MCR1) and V2HS (VIU_MCR2) when used as outputs 0 active low 1 active high
9	R/W	0	OBP Output Video Blank Polarity. Specifies polarity of horizontal/composite blanking signals V1BL (VIU_MCR1) and V2BL (VIU_MCR2) when used as outputs 0 active low 1 active high
8	R/W	0	OBT Output Video Blank Type. Specifies type of horizontal/composite blanking signals V1BL (VIU_MCR1) and V2BL (VIU_MCR2) when used as outputs 0 Hblank 1 Cblank
7	R/W	0	IFP Input Video Field Polarity 0 active low 1 active high

Bit #	Access	Res	Description (cont.)	
6	R/W	0	ISS	Input Sync Source 0 V1VS/V2VS, V1HS/V2HS, V1BL/V2BL input to CL-PX2070 1 V1VS/V2VS, V1HS/V2HS, V1BL/V2BL output from CL-PX2070
5	R/W	0	IVSP	Input Video VSync Polarity. Specifies polarity of vertical sync signals V1VS (VIU_MCR1) and V2VS (VIU_MCR2) when signals are used as input. 0 active low 1 active high
4	R/W	0	IHSP	Input Video Horizontal Sync Polarity. Specifies polarity of horizontal sync signals V1HS (VIU_MCR1) and V2HS (VIU_MCR2) when used as inputs. 0 active low 1 active high
3	R/W	0	IBP	Input Video Blank Polarity. Specifies polarity of horizontal/composite blanking signals V1BL (VIU_MCR1) and V2BL (VIU_MCR2) when used as inputs 0 active low 1 active high
2	R/W	0	IBT	Input Video Blank Type. Specifies type of horizontal/composite blanking signals V1BL (VIU_MCR1) and V2BL (VIU_MCR2) when used as inputs 0 HBlank 1 CBlank
1 0	R/W	00	IOM	Input/Output Mode. Specifies whether Video Port V1 or V2 is input only, output only, or duplexed under the control of V1PH (V1) or V2PH (V2) 00 Input only 11 Output only 10 Duplex, output on V1PH/V2PH high 11 Duplex, output on V1PH/V2PH low

4.2.1.2 VIU_DPC1: Datapath Control

I/O Address: VIU_RDT
Index: 1002 (VIU_DPC1 Datapath Control Field 1)
1003 (VIU_DPC2 Datapath Control Field 2)

Registers VIU_DPC1 and VIU_DPC2 specify the flow of stream data and the source of control sync references for the IPU1, the IPU2, and the OPU for fields 1 and 2

RSVD				VSUDC			IPU1DC			IPU2DC			ODC		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 12	R/W	0000	RSVD	Reserved (read as 0)
11 9	R/W	000	VSUDC	VSU Datapath Control 000 V1 sources clock 001 V1 sources clock, V1PH qualified 010 V2 sources clock 011 V2 sources clock, V2PH qualified 100 MCLK/3 timebase 101 MCLK/6 timebase 110, 111 Reserved
8 6	R/W	000	IPU1DC	IPU1 Datapath Control. Specifies the source of control sync references and input stream data for the IPU1 000 V1 sources control sync/data 001 V1 sources control sync/data, V1PH qualified 010 V2 sources control sync/data 011 V2 sources control sync/data, V2PH qualified 100 OPU sources data, MCLK/3 HS timebase, sync from VSU 101 OPU sources data, MCLK/6 HS timebase, sync from VSU 110, 111 Reserved
5 3	R/W	000	IPU2DC	IPU2 Datapath Control. Specifies the source of control sync references and input stream data for the IPU2 000 V1 sources control sync/data 001 V1 sources control sync/data, V1PH qualified 010 V2 sources control sync/data 011 V2 sources control sync/data, V2PH qualified 100 OPU sources data, MCLK/3[a] HS timebase, sync from VSU 101 OPU sources data, MCLK/6 HS timebase, sync from VSU 110 BIU sources control data, no sync controls 111 Reserved
2 0	R/W	000	ODC	OPU Datapath Control. Specifies the source of control sync references and the destination of output stream data from the OPU 000 V1 sources control sync 001 V1 sources control sync, V1PH qualified 010 V2 sources control sync 011 V2 sources control sync, V2PH qualified 100 VSU sources control sync, MCLK/3 timebase 101 VSU sources control sync, MCLK/6 timebase 110 BIU receives data, no sync controls 111 Reserved

a. MCLK/3 is expressed as "sequencer clock" in some other places in this document

4.2.1.3 *VIU_WDT: Watchdog Timer*

I/O Address: HIU BD1
Index: 1004

Register VIU_WDT controls the operation of the watchdog timer, and specifies the field toggle mode of the SIU.

RSVD	MMS	MFTS			WTE	TMOUT									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
15	R/W	0	RSVD	Reserved (read as 0)
14	R/W	0	MMS	Manual Mode Start. Writing 0, then 1 while *MFTS is programmed to 6h* initiates a field toggle in manual mode
13:11	R/W	000	MFTS	Master Field Toggle Select. Specifies the field toggle mode for the SIU. The field toggles on the leading edge of Vsync. 000 Field timing from V1 input video Vsync 001 Field timing from V1 output video Vsync 010 Field timing from V2 input video Vsync 011 Field timing from V2 output video Vsync 100 Field timing from watchdog timer 101 Field timing from VSU Vsync 110 Field timing from manual mode start 111 Reserved
10	R/W	0	WTE	Watchdog Timer Enable. Enables or disables the operation of the watchdog timer. 0 Disable watchdog timer 1 Enable watchdog timer
9:0	R/W	0h	TMOUT	Timeout. Specifies the watchdog timer interval. The timebase interval is the memory clock signal MCLK prescaled by a factor of 49,152 (3 * 214) (0 3FFh)

4.2.2 VSU: Video Sync Unit

The following sections describe the VSU registers, shown in Figure 4-1 and Figure 4-2.

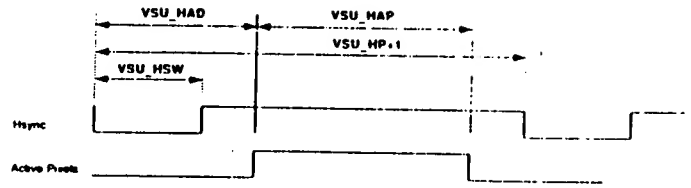

Figure 4-1. VSU Horizontal Sync Timing

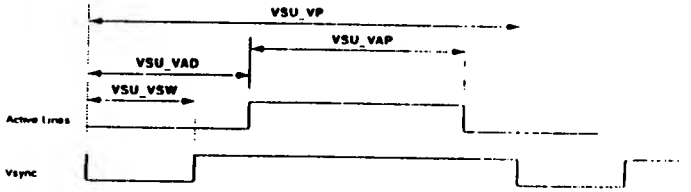

Figure 4-2. VSU Vertical Sync Timing

4.2.2.1 VSU_HSW: Horizontal Sync Width

I/O Address HIU_RDT
Index 1100

See also Figure 4-1 VSU Horizontal Sync Timing, p. 95

Register VSU_HSW specifies the width of the horizontal sync pulse generated by the internal sync generator. The timebase is specified by fields IPU1DC and IPU2DC of register VIU_DPCI.

RSVD									HSW							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Bit #	Access	Reset	Description	
15:7	R/W	0h	RSVD	Reserved (read as 0)
6:0	R/W	0h	HSW	Horizontal sync width (0-7Fh)

4.2.2.2 VSU_HAD: Horizontal Active Delay

I/O Address HIU_RDT
Index 1101

See also Figure 4-1 VSU Horizontal Sync Timing, p. 95

Register VSU_HAD specifies the delay from the start of the horizontal sync pulse generated by the internal sync generator to the beginning of the horizontal active interval. The timebase is specified by fields IPU1DC and IPU2DC of register VIU_DPCI.

RSVD						HAD									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:10	R/W	0h	RSVD	Reserved (read as 0)
9:0	R/W	0h	HAD	Horizontal active delay (0-3Ffh)

4.2.2.3 VSU_HAP: Horizontal Active Pixels

I/O Address HIU_RDT
Index 1102

See also Figure 4-1 VSU Horizontal Sync Timing, p. 95

Register VSU_HAP specifies the width of the horizontal active interval generated by the internal sync generator. The timebase is input memory clock signal MCLK prescaled by a factor of 3 or 6, as specified by fields IPU1DC and IPU2DC of register VIU_DPCI.

RSVD					HAP										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	HAP	Horizontal active pixels (0-3FFh)

4.2.2.4 VSU_HP: Horizontal Period

I/O Address HIU_RDT
Index 1103

See also Figure 4-1 VSU Horizontal Sync Timing, p. 95

Register VSU_HP specifies the width of the horizontal sync period generated by the internal sync generator. The timebase is input memory clock signal MCLK prescaled by a factor of 3 or 6, as specified by fields IPU1DC and IPU2DC of register VIU_DPCI.

NOTE: The number entered in HP must be one less than the desired interval. See Section 3.2.3 on page 43 for additional information.

RSVD						HP									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:10	R/W	0h	RSVD	Reserved (read as 0)
9:0	R/W	0h	HP	Desired horizontal period (0-3Ffh) - 1

4.2.2.5 VSU_VSW: Vertical Sync Width

I/O Address HIU_RDT
Index 1104

See also Figure 4-2 VSU Vertical Sync Timing, p. 95

Register VSU_VSW specifies the width of the vertical sync pulse generated by the internal sync generator. The timebase is the horizontal sync interval specified by register VSU_HP.

RSVD									VSW						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15-7	R/W	0h	RSVD	Reserved (read as 0)
6-0	R/W	0h	VSW	Vertical sync width (0-7Fh)

4.2.2.6 VSU_VAD: Vertical Active Delay

I/O Address HIU_RDT
Index 1105

See also Figure 4-2 VSU Vertical Sync Timing, p. 95

Register VSU_VAD specifies the delay from the start of the vertical sync pulse generated by the internal sync generator to the beginning of the vertical active interval. The timebase is the horizontal sync interval specified by register VSU_HP.

RSVD						VAD									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15-10	R/W	0h	RSVD	Reserved (read as 0)
9-0	R/W	0h	VAD	Vertical active delay (0-3FFh)

4.2.2.7 VSU_VAP: Vertical Active Pixels

I/O Address HIU_RDT
Index 1106

See also Figure 4-2 VSU Vertical Sync Timing, p. 95

Register VSU_VAP specifies the width of the vertical active interval generated by the internal sync generator. The timebase is the horizontal sync interval specified by register VSU_HP.

RSVD					VAP										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15-11	R/W	0h	RSVD	Reserved (read as 0)
10-0	R/W	0h	VAP	Vertical active pixels (0-7FFh)

4.2.2.8 VSU_VP: Vertical Period

I/O Address HIU_RDT
Index 1107

See also: Figure 4-2. VSU Vertical Sync Timing, p. 95

Register VSU_VP specifies the width of the vertical sync period generated by the internal sync generator. The timebase is the horizontal sync interval specified by register VSU_HP. This register also provides the enable and single sweep controls for the internal sync generator.

SGE	SSE	RSVD			VP										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	0	SGE	Sync Generator Enable
14	R/W	0	SSE	Single Sweep Enable - 1 Enables single sweep mode. When this bit is written as 1, SGE resets to 0 at the end of the sweep. When SGE is set (written as 1), another single sweep occurs after which it is reset.
13-10	R/W	0000	RSVD	Reserved (read as 0)
9-0	R/W	0h	VP	Vertical active count (0-7FFh)

4.3 VPU: Video Processor Unit — Registers

Table 4-5. VPU Registers Accessed by the Register Data Port

Name	Index	Definition	Ref. Section
VPU Global Control			4.3.1, page 105
VPU_MCR	2000	Master Control	4.3.1.1, page 105
IPU1: Input Processor Unit 1			4.3.2, page 106
IPU1_PIX	2100	Pixel Count	4.3.2.1, page 106
IPU1_LIC	2101	Line Count	4.3.2.2, page 106
IPU1_FLC	2102	Field Count	4.3.2.3, page 107
IPU1_LIR	2103	Line Count Interrupt Request	4.3.2.4, page 107
IPU1_FIR	2104	Field Count Interrupt Request	4.3.2.5, page 108
IPU1_LRB	2200	LUT RAM Base Address	4.3.2.6, page 108
IPU1_LRD	2201	LUT RAM Data	4.3.2.7, page 109
IPU1_MCR1	3000	Master Control Field 1	4.3.2.8, page 109
IPU1_XBF1	3001	X Begin Fraction Field 1	4.3.2.9, page 111
IPU1_XBI1	3002	X Begin Integer Field 1	4.3.2.9, page 111
IPU1_XEI1	3003	X End Integer Field 1	4.3.2.10, page 112
IPU1_XSF1	3004	X Shrink Fraction Field 1	4.3.2.11, page 113
IPU1_XSI1	3005	X Shrink Integer Field 1	4.3.2.11, page 113
IPU1_YBF1	3006	Y Begin Fraction Field 1	4.3.2.12, page 114
IPU1_YBI1	3007	Y Begin Integer Field 1	4.3.2.12, page 114
IPU1_YEI1	3008	Y End Integer Field 1	4.3.2.13, page 115
IPU1_YSF1	3009	Y Shrink Fraction Field 1	4.3.2.14, page 116
IPU1_YSI1	300a	Y Shrink Integer Field 1	4.3.2.14, page 116
IPU1_KFC1	300b	Key Function Code Field 1	4.3.2.15, page 117
IPU1_MMY1	300c	Chroma Key Y/R Max/Min Field 1	4.3.2.16, page 117
IPU1_MMU1	300d	Chroma Key U/G Max/Min Field 1	4.3.2.16, page 117
IPU1_MMV1	300e	Chroma Key V/B Max/Min Field 1	4.3.2.16, page 117
IPU1_MCR2	3100	Master Control Field 2	4.3.2.8, page 109
IPU1_XBF2	3101	X Begin Fraction Field 2	4.3.2.9, page 111

Table 4-5. VPU Registers Accessed by the Register Data Port *(cont.)*

Name	Index	Definition	Ref. Section
IPU1_XBI2	3102	X Begin Integer Field 2	4.3.2.9, page 111
IPU1_XEI2	3103	X End Integer Field 2	4.3.2.10, page 112
IPU1_XSF2	3104	X Shrink Fraction Field 2	4.3.2.11, page 113
IPU1_XSI2	3105	X Shrink Integer Field 2	4.3.2.11, page 113
IPU1_YBF2	3106	Y Begin Fraction Field 2	4.3.2.12, page 114
IPU1_YBI2	3107	Y Begin Integer Field 2	4.3.2.12, page 114
IPU1_YEI2	3108	Y End Integer Field 2	4.3.2.13, page 115
IPU1_YSF2	3109	Y Shrink Fraction Field 2	4.3.2.14, page 116
IPU1_YSI2	310a	Y Shrink Integer Field 2	4.3.2.14, page 116
IPU1_KFC2	310b	Key Function Code Field 2	4.3.2.15, page 117
IPU1_MMY2	310c	Chroma Key Y/R Max/Min Field 2	4.3.2.16, page 117
IPU1_MMU2	310d	Chroma Key U/G Max/Min Field 2	4.3.2.16, page 117
IPU1_MMV2	310e	Chroma Key V/B Max/Min Field 2	4.3.2.16, page 117
IPU2: Input Processor Unit 2			4.3.3, page 119
IPU2_PIX	2300	Pixel Count	4.3.3.1, page 119
IPU2_LIC	2301	Line Count	4.3.3.2, page 119
IPU2_FLC	2302	Field Count	4.3.3.3, page 120
IPU2_LIR	2303	Line Count Interrupt Request	4.3.3.4, page 120
IPU2_FIR	2304	Field Count Interrupt Request	4.3.3.5, page 121
IPU2_MCR1	3200	Master Control Field 1	4.3.3.6, page 121
IPU2_XBI1	3202	X Begin Integer Field 1	4.3.3.7, page 122
IPU2_XEI1	3203	X End Integer Field 1	4.3.3.8, page 122
IPU2_YBI1	3207	Y Begin Integer Field 1	4.3.3.9, page 123
IPU2_YEI1	3208	Y End Integer Field 1	4.3.3.10, page 123
IPU2_MCR2	3300	Master Control Field 2	4.3.3.6, page 121
IPU2_XBI2	3302	X Begin Integer Field 2	4.3.3.7, page 122
IPU2_XEI2	3303	X End Integer Field 2	4.3.3.8, page 122
IPU2_YBI2	3307	Y Begin Integer Field 2	4.3.3.9, page 123

Table 4-5. VPU Registers Accessed by the Register Data Port *(cont.)*

Name	Index	Definition	Ref. Section
IPU2_YEI2	3308	Y End Integer Field 2	4.3.3.10, page 123
SIU: Sequencer Instruction Unit			4.3.4, page 124
SIU_MCR	2800	Master Control	4.3.4.1, page 124
SIU_FCS	2801	FIFO Control/Status	4.3.4.2, page 124
SIU_FOU	2802	FIFO Overflow/Underflow	4.3.4.2, page 124
SIU0_SIM	2e00	Sequencer Instruction Memory 0	4.3.4.4, page 127
SIU1_SIM	2e01	Sequencer Instruction Memory 1	4.3.4.4, page 127
SIU2_SIM	2e02	Sequencer Instruction Memory 2	4.3.4.4, page 127
SIU3_SIM	2e03	Sequencer Instruction Memory 3	4.3.4.4, page 127
SIU4_SIM	2e04	Sequencer Instruction Memory 4	4.3.4.4, page 127
SIU5_SIM	2e05	Sequencer Instruction Memory 5	4.3.4.4, page 127
SIU6_SIM	2e06	Sequencer Instruction Memory 6	4.3.4.4, page 127
SIU7_SIM	2e07	Sequencer Instruction Memory 7	4.3.4.4, page 127
SIU8_SIM	2e08	Sequencer Instruction Memory 8	4.3.4.4, page 127
SIU9_SIM	2e09	Sequencer Instruction Memory 9	4.3.4.4, page 127
SIU10_SIM	2e0a	Sequencer Instruction Memory 10	4.3.4.4, page 127
SIU11_SIM	2e0b	Sequencer Instruction Memory 11	4.3.4.4, page 127
SIU12_SIM	2e0c	Sequencer Instruction Memory 12	4.3.4.4, page 127
SIU13_SIM	2e0d	Sequencer Instruction Memory 13	4.3.4.4, page 127
SIU14_SIM	2e0e	Sequencer Instruction Memory 14	4.3.4.4, page 127
SIU15_SIM	2e0f	Sequencer Instruction Memory 15	4.3.4.4, page 127
SIU16_SIM	2e10	Sequencer Instruction Memory 16	4.3.4.4, page 127
SIU17_SIM	2e11	Sequencer Instruction Memory 17	4.3.4.4, page 127
SIU18_SIM	2e12	Sequencer Instruction Memory 18	4.3.4.4, page 127
SIU19_SIM	2e13	Sequencer Instruction Memory 19	4.3.4.4, page 127
SIU20_SIM	2e14	Sequencer Instruction Memory 20	4.3.4.4, page 127
SIU21_SIM	2e15	Sequencer Instruction Memory 21	4.3.4.4, page 127
SIU22_SIM	2e16	Sequencer Instruction Memory 22	4.3.4.4, page 127

Table 4-5. VPU Registers Accessed by the Register Data Port *(cont.)*

Name	Index	Definition	Ref. Section
SIU23_SIM	2e17	Sequencer Instruction Memory 23	4.3.4.4, page 127
SIU24_SIM	2e18	Sequencer Instruction Memory 24	4.3.4.4, page 127
SIU25_SIM	2e19	Sequencer Instruction Memory 25	4.3.4.4, page 127
SIU26_SIM	2e1a	Sequencer Instruction Memory 26	4.3.4.4, page 127
SIU27_SIM	2e1b	Sequencer Instruction Memory 27	4.3.4.4, page 127
SIU28_SIM	2e1c	Sequencer Instruction Memory 28	4.3.4.4, page 127
SIU29_SIM	2e1d	Sequencer Instruction Memory 29	4.3.4.4, page 127
SIU30_SIM	2e1e	Sequencer Instruction Memory 30	4.3.4.4, page 127
SIU31_SIM	2e1f	Sequencer Instruction Memory 31	4.3.4.4, page 127
ALU: Arithmetic and Logic Unit			4.3.5, page 128
ALU_MCR1	2900	Master Control Field 1	4.3.5.1, page 128
ALU_MCR2	2901	Master Control Field 2	4.3.5.1, page 128
ALU_TOP	2902	Tag Operation	4.3.5.2, page 129
ALU_AV	2903	Alpha Value	4.3.5.3, page 130
ALU_LOPY	2904	Logic Operation Channel Y	4.3.5.4, page 130
ALU_LOPU	2905	Logic Operation Channel U	4.3.5.4, page 130
ALU_LOPV	2906	Logic Operation Channel V	4.3.5.4, page 130
ALU_CAY	2907	Constant A, Channel Y	4.3.5.5, page 131
ALU_CAU	2908	Constant A, Channel U	4.3.5.5, page 131
ALU_CAV	2909	Constant A, Channel V	4.3.5.5, page 131
ALU_CBY	290a	Constant B, Channel Y	4.3.5.6, page 131
ALU_CBU	290b	Constant B, Channel U	4.3.5.6, page 131
ALU_CBV	290c	Constant B, Channel V	4.3.5.6, page 131
ALU_CCY	290d	Constant C, Channel Y	4.3.5.7, page 132
ALU_CCU	290e	Constant C, Channel U	4.3.5.7, page 132
ALU_CCV	290f	Constant C, Channel V	4.3.5.7, page 132

Table 4-5. VPU Registers Accessed by the Register Data Port *(cont.)*

Name	Index	Definition	Ref. Section
OPU: Output Processing Unit			
OPU_MCR1	2a00	Master Control Field 1	4.3.6, page 133
OPU_XB11	2a02	X Begin Integer Field 1	4.3.6.1, page 133
OPU_XE11	2a03	X End Integer Field 1	4.3.6.2, page 134
OPU_YB11	2a07	Y Begin Integer Field 1	4.3.6.3, page 134
OPU_YE11	2a08	Y End Integer Field 1	4.3.6.4, page 135
OPU_MCR2	2b00	Master Control Field 2	4.3.6.5, page 135
OPU_XB12	2b02	X Begin Integer Field 2	4.3.6.1, page 133
OPU_XE12	2b03	X End Integer Field 2	4.3.6.2, page 134
OPU_YB12	2b07	Y Begin Integer Field 2	4.3.6.3, page 134
OPU_YE12	2b08	Y End Integer Field 2	4.3.6.4, page 135
			4.3.6.5, page 135

4.3.1 VPU Global Control

4.3.1.1 VPU_MCR: Master Control

I/O Address HIU_RDT
Index 2000

Register VPU_MCR controls the operation of the IPU1, the IPU2, and the OPU for fields 1 and 2.

RSVD			ALUE	OPFSS				IP2FSS				IP1FSS			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15.13	R/W	0h	RSVD	Reserved (read as 0)
12	R/W	0	ALUE	ALU Enable. Enables or disables the operation of the ALU. 0 Disable ALU operation 1 Enable ALU operation
11.8	R/W	0000	OPFSS	OPU Field Sync Select. Enables or disables the operation of the OPU, specifies whether it processes one or both fields, and specifies the field synchronization. 0000 Disable unit operation 0001 Start unit on next field, both fields 0010 Start unit on field 1, single field only 0011 Start unit on field 1, both fields 0100 Start unit on field 2, single field only 0101 Start unit on field 2, both fields
7.4	R/W	0000	IP2FSS	IPU2 Field Sync Select. Enables or disables the operation of the IPU2, specifies whether it processes one or both fields, and specifies the field synchronization. 0000 Disable unit operation 0001 Start unit on next field, both fields 0010 Start unit on field 1, single field only 0011 Start unit on field 1, both fields 0100 Start unit on field 2, single field only 0101 Start unit on field 2, both fields
3.0	R/W	0000	IP1FSS	IPU1 Field Sync Select. Enables or disables the operation of the IPU1, specifies whether it processes one or both fields, and specifies the field synchronization. 0000 Disable unit operation 0001 Start unit on next field, both fields 0010 Start unit on field 1, single field only 0011 Start unit on field 1, both fields 0100 Start unit on field 2, single field only 0101 Start unit on field 2, both fields

4.3.2 IPU1: Input Processor Unit 1

4.3.2.1 *IPU1_PIX: Pixel Count*

I/O Address HIU_RDT
Index 2100

Register IPU1_PIX is a read only register that reads back the value of the current 11 bit pixel counter. It automatically resets to 0 at the beginning of each line

RSVD					PC										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 11	Read Only	0h	RSVD	Reserved (read as 0)
10 0	Read Only	0h	PC	Pixel Count current line (0 7FFh)

4.3.2.2 *IPU1_LIC: Line Count*

I/O Address HIU_RDT
Index 2101

Register IPU1_LIC is a read only register of the current 11 bit line count. It automatically resets to 0 at the beginning of each field

RSVD					LC										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 11	Read Only	0h	RSVD	Reserved (read as 0)
10 0	Read Only	0h	LC	Line Count current field (0 7FFh)

4.3.2.3 *IPU1_FLC: Field Count*

I/O Address HIU_RDT
Index 2102

Register IPU1_FLC returns the current 15 bit field count on read, is set to zero when bit FCE in IPU1_FIFI is set to zero.

RSVD	FC														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	Read Only	0h	RSVD	Reserved (read as 0)
15 0	Read Only	0h	FC	Field Count

4.3.2.4 *IPU1_LIR: Line Count Interrupt Request*

I/O Address HIU_RDT
Index 2103

Register IPU1_LIR generates an interrupt request when the 11 bit value in field IRLC is equal to the value in field LC of register IPU1_LIC.

RSVD					IRLC										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 11	R/W	0h	RSVD	Reserved (read as 0)
10 0	R/W	0h	IRLC	Interrupt Request Line Count (0 7FFh)

4.3.2.5 IPU1_FIR: Field Count Interrupt Request

I/O Address HIU_RDT
Index 2104

Register IPU1_FIR generates an interrupt request when the 15 bit value in field IRFC is equal to the value in field FC of register IPU1_FLC.

FCE	IRFC														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	0h	FCE	Field Count Enable 1 field count enabled 0 field count disabled
14 0	R/W	0h	IRFC	Interrupt Request Field Count

4.3.2.6 IPU1_LRB: LUT RAM Base Address

I/O Address HIU_RDT
Index 2200

Register IPU1_LRB preloads the 8 bit LUT RAM address counter and initializes the channel pointer to the YR channel. The channel pointer automatically advances to the next channel after each LUT RAM access, and address counter automatically increments after accessing the CrB channel. LUT RAM elements are accessed in the following order: YR[LRB+0], CbG[LRB+0], CrB[LRB+0], YR[LRB+1], CbG[LRB+1], CrB[LRB+1], etc.

RSVD								LRB							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 8	R/W	0h	RSVD	Reserved (read as 0)
7 0	R/W	0h	LRB	LUT RAM Base Address. Specifies the 8 bit address generator preload value (0 FFh)

4.3.2.7 IPU1_LRD: LUT RAM Data

I/O Address HIU_RDT
Index 2201

See also IPU1_LRB LUT RAM Base Address, p. 108

Register IPU1_LRD is the bidirectional data port to the storage elements of the three channel LUT RAM.

RSVD								LRD							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 8	R/W	0h	RSVD	Reserved (read as 0)
7 0	R/W	0h	LRD	LUT RAM Data. Data written to this field transfers to the current LUT RAM element; data to be read from the current LUT RAM element appears in this field. (0 FFh)

4.3.2.8 IPU1_MCR1: Master Control

I/O Address HIU_RDT
Index 3000 (IPU1_MCR1 Master Control Field 1)
3100 (IPU1_MCR2 Master Control Field 2)

See also Special Y Scaling Path Mode, p. 57
IPU1, Input Processor Unit 1, Section 3.3.2 on page 50
Figure 3-16 IPU1 Input Processor Unit 1, p. 51

Registers IPU1_MCR1 and IPU1_MCR2 control the operation of the IPU1 for fields 1 and 2.

FPS	IM	PSE	CSCE	LE	YSP	ODT		OF				IF			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	0	FPS	Field Polarity Select. Controls the polarity of the field ID signal supplied to the Window Clipping and XY Scaler. 0 Normal polarity 1 Invert polarity
14	R/W	0	IM	Interlace Mode. Specifies the input stream as interlaced or non interlaced data. 0 Progressive scan input 1 Interlaced input

Bit #	Access	Reset	Description *(cont.)*	
13	R/W	0	PSE	Prescaler Enable. Enables or disables the operation of the X Prescaler. 0 Bypass prescaler 1 Enable 0.5 X prescaler
12	R/W	0	CSCE	Color Space Converter Enable. Enables or disables the operation of the Color Space Converter. 0 Bypass color space converter 1 Enable color space converter
11	R/W	0	LE	LUT Enable. Enables or disables the operation of the LUT RAM. 0 Bypass LUT RAM 1 Enable LUT RAM
10	R/W	0	YSP	Y Scaling Path. Enables or disables the special Y Scaling Path Mode. 0 Y Scaler performs Y scaling 1 ALU performs Y scaling
9:8	R/W	00	ODT	Output Data Tag. Controls the input selection of the Input Tag Unit tag multiplexor (see Figure 3-27). 00 Pass tag unchanged 01 Set tag to field ID 10 Set tag to inverse chroma key tag 11 Set tag to chroma key tag
7:4	R/W	0000	OF	Output Data Format. Specifies the format of the output stream. 0000 YCbCr 4:2:2 non-tagged data 0001 YCbCr 4:2:2 tagged data 1000 RGB 5:6:5 non-tagged data 1001 RGB 1:5:5:5 tagged data 1010 RGB 8:8:8 non-tagged data 1011 RGB 1:8:8:8 tagged data 1110 RGB 3:3:2 non-tagged data
3:0	R/W	0000	IF	Input Data Format. Specifies the format of the input stream. 0000 YCbCr 4:2:2 non-tagged data 0001 YCbCr 4:2:2 tagged data 0010 YCbCr 4:1:1 non-tagged data 1000 RGB 5:6:5 non-tagged data 1001 RGB 1:5:5:5 tagged data 1110 Pseudo color (indirect color mapping via IPU1 LUT)

4.3.2.9 IPU1_XBnI: X Begin

I/O Address: HIU_RDT
Index: 3001 (IPU1_XBF1 X Begin Fraction Field 1)
3002 (IPU1_XBI1 X Begin Integer Field 1)
3101 (IPU1_XBF2 X Begin Fraction Field 2)
3102 (IPU1_XBI2 X End Integer Field 2)

See also: Section 3.3.2 on page 50
Section 3.3.2.5 on page 56

Registers IPU1_XBnI specify the 11.3 format X begin value for fields 1 and 2.

X Begin Fraction Index (IPU1_XBF1 and IPU1_XBF2)

IPU1_XBF1 and IPU1_XBF2 allow the virtual left boundary of the post scaled window to be aligned between pixels of the pre-scaled window for fields 1 and 2.

BF			RSVD												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:13	R/W	0h	BF	Begin X Column Fractional Index. Specifies the 3 bit fractional portion of the 11.3 format X begin value (0.7h).
12:0	R/W	0h	RSVD	Reserved (read as 0)

X Begin Integer Index (IPU1_XBI1 and IPU1_XBI2)

Registers IPU1_XBI1 and IPU1_XBI2 define the left boundary of the pre scaling window for fields 1 and 2. All video to the left of this boundary is clipped and is not used to generate the scaled window.

RSVD					BI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	BI	Begin X Column Integer Index. Specifies the 11 bit integer portion of the 11.3 format X begin value (0.7FFh).

4.3.2.10 IPU1_XEfl: X End

I/O Address HIU_RDT
Index 3003 (IPU1_XEf1: X End Integer Field 1)
3103 (IPU1_XEf2: X End Integer Field 2)

See also Figure 3-18 Window Clipping and XY Scaling Control Registers, p. 56

Registers IPU1_XEf1 and IPU1_XEf2 specify the 11 bit X end value for fields 1 and 2.

RSVD					EI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	EI	X End Column Integer Index. Specifies the 11-bit X end value (0-7FFh)

4.3.2.11 IPU1_XSnf: X Shrink

I/O Address HIU_RDT
Index 3004 (IPU1_XSF1: X Shrink Fraction Field 1)
3005 (IPU1_XSI1: X Shrink Integer Field 1)
3104 (IPU1_XSF2: X Shrink Fraction Field 2)
3105 (IPU1_XSI2: X Shrink Integer Field 2)

See also Figure 3-18 Window Clipping and XY Scaling Control Registers, p. 56

Registers IPU1_XSnf specify the 6.10 format X shrink value for fields 1 and 2.

X Shrink Fraction (IPU1_XSF1 and IPU1_XSF2)

SF										RSVD					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:5	R/W	0h	SF	X Shrink Fraction. Specifies the 10-bit fractional portion of the 6.10 format X shrink value (0-3FFh)
4:0	R/W	0h	RSVD	Reserved (read as 0)

X Shrink Integer (IPU1_XSI1 and IPU1_XSI2)

RSVD										SI					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:6	R/W	0h	RSVD	Reserved (read as 0)
5:0	R/W	0h	SI	X Shrink Integer. Specifies the 4-bit integer portion of the 4.10 format X shrink value (0-Fh)

4.3.2.12 IPU1_YBnf: Y Begin

I/O Address IIIU_RDT
Index 3006 (IPU1_YBF1 Y Begin)
3007 (IPU1_YBI1 Y Begin)
3106 (IPU1_YBF2 Y Begin)
3107 (IPU1_YBI2 Y Begin)

See also Figure 3-18 Window Clipping and XY Scaling Control Registers, p. 56

Registers IPU1_YBnI specify the 11.3 format Y begin value for fields 1 and 2.

Y Begin Fraction Index (IPU1_YBF1 and IPU1_YBF2)

Registers IPU1_YBF1 and IPU1_YBF2 allow the virtual top row of the post-scaled window to be aligned between rows of the pre-scaled window for fields 1 and 2

BF			RSVD												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:13	R/W	0h	BF	Begin Y Row Fractional Index: Specifies the 3 bit fractional portion of the 11.3 format Y begin value (0-7h)
12:0	R/W	0h	RSVD	Reserved (read as 0)

Y Begin Integer Index (IPU1_YBI1 and IPU1_YBI2)

Registers IPU1_YBI1 and IPU1_YBI2 define the top edge of the pre-scaling window for fields 1 and 2. All video above this boundary is clipped and does not become part of the scaled window.

RSVD					BI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	BI	Begin Y Row Integer Index: Specifies the 11 bit integer portion of the 11.3 format Y begin value (0-7FFh)

4.3.2.13 IPU1_YEIf: Y End

I/O Address IIIU_RDT
Index 3008 (IPU1_YEI1 Y End Integer Field 1)
3108 (IPU1_YEI2 Y End Integer Field 2)

See also Figure 3-18 Window Clipping and XY Scaling Control Registers, p. 56

Registers IPU1_YEI1 and IPU1_YEI2 specify the 11 bit Y end value for fields 1 and 2

RSVD					EI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	EI	End Y Row Integer Index: Specifies the 11 bit Y end value (0-7FFh)

4.3.2.14 IPU1_YSnf: Y Shrink

I/O Address: HIU_RDT
Index:
- 3009 (IPU1_YSF1: Y Shrink Fraction Field 1)
- 300a (IPU1_YSI1: Y Shrink Integer Field 1)
- 3109 (IPU1_YSF2: Y Shrink Fraction Field 2)
- 310a (IPU1_YSI2: Y Shrink Integer Field 2)

See also: Figure 3-18, Window Clipping and XY Scaling Control Registers, p. 56

Registers IPU1_YSnf specify the 4.10 format Y shrink value for fields 1 and 2.

Y Shrink Fraction (IPU1_YSF1 and IPU1_YSF2)

SF										RSVD					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:6	R/W	0h	SF	Y Shrink Fraction. Specifies the 10 bit fractional portion of the 4.10 format Y shrink value (0-3FFh)
5:0	R/W	0h	RSVD	Reserved (read as 0)

Y Shrink Integer (IPU1_YSI1 and IPU1_YSI2)

RSVD										SI					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:6	R/W	0h	RSVD	Reserved (read as 0)
5:0	R/W	0h	SI	Y Shrink Integer. Specifies the 4-bit integer portion of the 4.10 format Y shrink value (0-Fh)

4.3.2.15 IPU1_KFC1: Key Function Code

I/O Address: HIU_RDT
Index:
- 300b (IPU1_KFC1: Key Function Code Field 1)
- 310b (IPU1_KFC2: Key Function Code Field 2)

See also: Figure 3-17, Input Tag Unit, p. 55

Registers IPU1_KFC1 and IPU1_KFC2 specify eight 1 bit values used by the key function code multiplexers for fields 1 and 2.

RSVD								KEYFC							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:8	R/W	0h	RSVD	Reserved (read as 0)
7:0	R/W	0h	KEYFC	Key Function Code. Specifies eight 1 bit input values used by the key function code multiplexers (0-FFh)

4.3.2.16 IPU1_MMxf: Chroma Key Max/Min

I/O Address: HIU_RDT
Index:
- 300c (IPU1_MMY1: Chroma Key Y/R Max/Min Field 1)
- 300d (IPU1_MMU1: Chroma Key U/G Max/Min Field 1)
- 300e (IPU1_MMV1: Chroma Key V/B Max/Min Field 1)
- 310c (IPU1_MMY2: Chroma Key Y/R Max/Min Field 2)
- 310d (IPU1_MMU2: Chroma Key U/G Max/Min Field 2)
- 310e (IPU1_MMV2: Chroma Key V/B Max/Min Field 2)

Registers IPU1_MMxf specify the maximum and minimum 8 bit chroma key comparator values used by the Input Tag Unit for fields 1 and 2. These values are used for each of three 8 bit input channels for both fields 1 and 2 (see Figure 3-27).

Key Y/R Maximum/Minimum (IPU1_MMY1 and IPU1_MMY2)

YRMAX								YRMIN							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:8	R/W	0h	YRMAX	Key Y/R Maximum. Specifies the upper threshold for the 8 bit Y (YCbCr stream) or R (RGB stream) channel comparator. (0-FFh)
7:0	R/W	0h	YRMIN	Key Y/R Minimum. Specifies the lower threshold for the 8-bit Y (YCbCr stream) or R (RGB stream) channel comparator. (0-FFh)

Key U/G Maximum/Minimum (IPU1_MMU1 and IPU1_MMU2)

UGMAX								UGMIN							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:8	R/W	0h	UGMAX	Key U/G Maximum. Specifies the upper threshold for the 8 bit Cb (YCb-Cr stream) or G (RGB stream) channel comparator. (0-FFh)
7:0	R/W	0h	UGMIN	Key U/G Minimum. Specifies the lower threshold for the 8 bit Cb (YCb-Cr stream) or G (RGB stream) channel comparator. (0-FFh)

Key V/B Maximum/Minimum (IPU1_MMV1 and IPU1_MMV2)

VBMAX								VBMIN							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:8	R/W	0h	VBMAX	Key V/B Maximum. Specifies the upper threshold for the 8 bit Cr (YCb-Cr stream) or B (RGB stream) channel comparator. (0-FFh)
7:0	R/W	0h	VBMIN	Key V/B Minimum. Specifies the lower threshold for the 8 bit Cr (YCbCr stream) or B (RGB stream) channel comparator. (0-FFh)

4.3.3 IPU2: Input Processing Unit 2

4.3.3.1 IPU2_PIX: Pixel Count

I/O Address HIU_RDT
Index 2300

Register IPU2_PIX is a read-only register of the current 11 bit pixel count. It automatically resets to 0 at the beginning of each line.

RSVD					PC										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	Read Only	0h	RSVD	Reserved (read as 0)
10:0	Read Only	0h	PC	Pixel Count current line (0-7FFh)

4.3.3.2 IPU2_LIC: Line Count

I/O Address HIU_RDT
Index 2301

Register IPU2_LIC is a read-only register of the current 11 bit line count. It automatically resets to 0 at the beginning of each field.

RSVD					LC										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	Read Only	0h	RSVD	Reserved (read as 0)
10:0	Read Only	0h	LC	Line Count current field (0-7FFh)

4.3.3.3 IPU2_FLC: Field Count

I/O Address HIU_RDT
Index 2302

On read, register IPU2_FLC returns the current 15 bit field count.

RSVD	FC													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	Read Only	0h	RSVD	Reserved (read as 0)
14 0	Read Only	0h	FC	Field count

4.3.3.4 IPU2_LIR: Line Count Interrupt Request

I/O Address HIU_RDT
Index 2303

Register IPU2_LIR specifies an 11 bit line count value that generates an interrupt request when equal to the realtime line count value in register IPU2_LIC.

RSVD					IRLC										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	0h	RSVD	Reserved (read as 0)
0	R/W	0h	IRLC	Interrupt Request Line Count (0 7FFh)

4.3.3.5 IPU2_FIR: Field Count Interrupt Request

I/O Address HIU_RDT
Index 2304

Register IPU2_FIR specifies a 16-bit field count value that generates an interrupt request when equal to the realtime field count value in register IPU2_FLC.

FCE	IRFC														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	0	FCE	Field Count Enable 1 field count enable 0 field count disabled
14 0	R/W	0h	IRFC	Interrupt Request Field Count

4.3.3.6 IPU2_MCR1: Master Control

I/O Address HIU_RDT
Index 3200 (IPU2_MCR1: Master Control Field 1)
3300 (IPU2_MCR2: Master Control Field 2)

See also Figure 3-19 Input Processing Unit 2, p 60
Figure 3-21. IPU2 Window Clipping Unit, p 62

Registers IPU2_MCR1 and IPU2_MCR2 control the operation of the IPU2

FPS	IM	PSE	RSVD												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	0h	FPS	Field Polarity Select Controls the polarity of the field ID signal supplied to the XY Window Clipping subunit 0 Normal polarity 1 Invert polarity
14	R/W	0h	IM	Interlace Mode Specifies the input stream as interlaced or non interlaced data 0 Progressive scan input 1 Interlaced input
13	R/W	0h	PSE	Prescaler Enable Enables or disables the operation of the X Prescaler 0 Bypass prescaler 1 Enable 0 5 X prescaler
12 0	R/W	0h	RSVD	Reserved (read as 0)

4.3.3.7 IPU2_XBI1: X Begin

I/O Address HIU_RDT
Index 3202 (IPU2_XBI1: X Begin Integer Field 1)
3302 (IPU2_XBI2: X Begin Integer Field 2)

See also Figure 3-21. IPU2 Window Clipping Unit, p. 62

Registers IPU2_XBI1 and IPU2_XBI2 specify the 11 bit X begin value for fields 1 and 2.

RSVD					BI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	BI	Begin X Column Integer Index. Specifies the 11 bit integer portion of the 11.0 format X begin value (0-7FFh)

4.3.3.8 IPU2_XEI1: X End

I/O Address HIU_RDT
Index 3203 (IPU2_XEI1: X End Integer Field 1)
3303 (IPU2_XEI2: X End Integer Field 2)

See also Figure 3-21. IPU2 Window Clipping Unit, p. 62

Registers IPU2_XEI1 and IPU2_XEI2 specify the 11 bit X end value for fields 1 and 2.

RSVD					EI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	EI	End X Column Integer Index. Specifies the 11 bit X end value (0-7FFh)

4.3.3.9 IPU2_YBI1: Y Begin

I/O Address HIU_RDT
Index 3207 (IPU2_YBI1: Y Begin Integer Field 1)
3307 (IPU2_YBI2: Y Begin Integer Field 2)

See also Figure 3-21. IPU2 Window Clipping Unit, p. 62

Registers IPU2_YBI1 and IPU2_YBI2 specify the 11 bit Y begin value for fields 1 and 2

RSVD					BI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	BI	Begin Y Row Integer Index. Specifies the 11 bit integer portion of the 11 bit Y begin value (0-7FFh)

4.3.3.10 IPU2_YEI1: Y End

I/O Address HIU_RDT
Index 3208 (IPU2_YEI1: Y End Integer Field 1)
3308 (IPU2_YEI2: Y End Integer Field 2)

See also Figure 3-21. IPU2 Window Clipping Unit, p. 62

Registers IPU2_YEI1 and IPU2_YEI2 specify the 11-bit Y end value for fields 1 and 2

RSVD					EI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	EI	End Y Row Integer Index. Specifies the 11 bit Y end value (0-7FFh)

4.3.4 SIU: Sequencer Instruction Unit

4.3.4.1 SIU_MCR: Master Control

I/O Address HIU_RDT
Index 2800

Register SIU_MCR controls the operation of the SIU for fields 1 and 2.

RSVD		SE		FT		SI2					SI1				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 14	R/W	0h	RSVD	Reserved (read as 0)
13 12	R/W	00	SE	Sequencer Enable. Enables or disables the operation of the SIU 00 SIU halted 10 SIU enabled, start on SI1 11 SIU enabled, start on SI2
11 10	R/W	00	FT	Field Toggle. Specifies the field toggle mode and the association of the start index values to a field 00 No field toggle (SI1 is used, SI2 is ignored) 01 SI1 and SI2 toggle on vertical sync, no field association 10 Field 1 is associated to SI1, and fields 1 and 2 toggle on vertical sync 11 Field 1 is associated to SI2, and fields 1 and 2 toggle on vertical sync
9 5	R/W	0h	SI2	Start Index 2. Specifies the 5 bit sequencer instruction start index 2. (0-1Fh)
4 0	R/W	0h	SI1	Start Index 1. Specifies the 5 bit sequencer instruction start index 1. (0-1Fh)

4.3.4.2 SIU_FCS: FIFO Control/Status

I/O Address HIU_RDT
Index 2801

Register SIU_FCS is a special read/write register that provides realtime access to the full and empty flags from FIFOs A-G. All flags are active high. Writing a 1 to FIFO Empty Flag fields resets the corresponding FIFOs. Writing a 0 to FIFO Empty Flag fields enables the corresponding FIFOs.

RSVD		FGF	FGE	FFF	FFE	FEF	FEE	FDF	FDE	FCF	FCE	FBF	FBE	FAF	FAE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 14	R/W	0h	RSVD	Reserved (read as 0)
13	Rd-only	0h	FGF	FIFO G Full Flag
12	R/W	0h	FGE	FIFO G Empty Flag On read: empty flag On write: FIFO reset
11	Rd-only	0h	FFF	FIFO F Full Flag
10	R/W	0h	FFE	FIFO F Empty Flag On read: empty flag On write: FIFO reset
9	Rd-only	0h	FEF	FIFO E Full Flag
8	R/W	0h	FEE	FIFO E Empty Flag On read: empty flag On write: FIFO reset
7	Rd-only	0h	FDF	FIFO D Full Flag
6	R/W	0h	FDE	FIFO D Empty Flag On read: empty flag On write: FIFO reset
5	Rd-only	0h	FCF	FIFO C Full Flag
4	R/W	0h	FCE	FIFO C Empty Flag On read: empty flag On write: FIFO reset
3	Rd-only	0h	FBF	FIFO B Full Flag
2	R/W	0h	FBE	FIFO B Empty Flag On read: empty flag On write: FIFO reset
1	Rd-only	0h	FAF	FIFO A Full Flag
0	R/W	0h	FAE	FIFO A Empty Flag On read: empty flag On write: FIFO reset

4.3.4 SIU: Sequencer Instruction Unit

4.3.4.1 SIU_MCR: Master Control

I/O Address HIU_RDT
Index 2800

Register SIU_MCR controls the operation of the SIU for fields 1 and 2.

RSVD		SE		FT		SI2					SI1				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 14	R/W	0h	RSVD	Reserved (read as 0)
13 12	R/W	00	SE	Sequencer Enable. Enables or disables the operation of the SIU. 00 SIU halted 10 SIU enabled, start on SI1 11 SIU enabled, start on SI2
11 10	R/W	00	FT	Field Toggle. Specifies the field toggle mode and the association of the start index values to a field. 00 No field toggle (SI1 is used, SI2 is ignored) 01 SI1 and SI2 toggle on vertical sync, no field association 10 Field 1 is associated to SI1, and fields 1 and 2 toggle on vertical sync 11 Field 1 is associated to SI2, and fields 1 and 2 toggle on vertical sync
9 5	R/W	0h	SI2	Start Index 2. Specifies the 5 bit sequencer instruction start index 2 (0-1Fh)
4 0	R/W	0h	SI1	Start Index 1. Specifies the 5 bit sequencer instruction start index 1 (0-1Fh)

4.3.4.2 SIU_FCS: FIFO Control/Status

I/O Address HIU_RDT
Index 2801

Register SIU_FCS is a special read/write register that provides realtime access to the full and empty flags from FIFOs A-G. All flags are active high. Writing a 1 to FIFO Empty Flag fields resets the corresponding FIFOs. Writing a 0 to FIFO Empty Flag fields enables the corresponding FIFOs.

RSVD		FGF	FGE	FFF	FFE	FEF	FEE	FDF	FDE	FCF	FCE	FBF	FBE	FAF	FAE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 14	R/W	0h	RSVD	Reserved (read as 0)
13	Rd only	0h	FGF	FIFO G Full Flag
12	R/W	0h	FGE	FIFO G Empty Flag On read: empty flag On write: FIFO reset
11	Rd only	0h	FFF	FIFO F Full Flag
10	R/W	0h	FFE	FIFO F Empty Flag On read: empty flag On write: FIFO reset
9	Rd only	0h	FEF	FIFO E Full Flag
8	R/W	0h	FEE	FIFO E Empty Flag On read: empty flag On write: FIFO reset
7	Rd only	0h	FDF	FIFO D Full Flag
6	R/W	0h	FDE	FIFO D Empty Flag On read: empty flag On write: FIFO reset
5	Rd only	0h	FCF	FIFO C Full Flag
4	R/W	0h	FCE	FIFO C Empty Flag On read: empty flag On write: FIFO reset
3	Rd only	0h	FBF	FIFO B Full Flag
2	R/W	0h	FBE	FIFO B Empty Flag On read: empty flag On write: FIFO reset
1	Rd only	0h	FAF	FIFO A Full Flag
0	R/W	0h	FAE	FIFO A Empty Flag On read: empty flag On write: FIFO reset

4.3.4.3 SIU_FOU: FIFO Overflow/Underflow

I/O Address HIU_RDT
Index 2802

Register SIU_FOU is a read only register that provides realtime access to the overflow and underflow flags from FIFOs A-G. All flags are active high (overflow, underflow = 1).

RSVD		FGO	FGU	FFO	FFU	FEO	FEU	FDO	FDU	FCO	FCU	FBO	FBU	FAO	FAU
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 14	Rd only	0h	RSVD	RSVD Reserved (read as 0)
13	Rd only	0h	FGO	FGO FIFO G Overflow Flag (write 0 to clear), 0-1h
12	Rd only	0h	FGU	FGU FIFO G Underflow Flag (write 0 to clear), 0-1h
11	Rd only	0h	FFO	FFO FIFO F Overflow Flag (write 0 to clear), 0-1h
10	Rd only	0h	FFU	FFU FIFO F Underflow Flag (write 0 to clear), 0-1h
9	Rd only	0h	FEO	FEO FIFO E Overflow Flag (write 0 to clear); 0-1h
8	Rd only	0h	FEU	FEU FIFO E Underflow Flag (write 0 to clear), 0-1h
7	Rd only	0h	FDO	FDO FIFO D Overflow Flag (write 0 to clear); 0-1h
6	Rd only	0h	FDU	FDU FIFO D Underflow Flag (write 0 to clear); 0-1h
5	Rd only	0h	FCO	FCO FIFO C Overflow Flag (write 0 to clear), 0-1h
4	Rd only	0h	FCU	FCU FIFO C Underflow Flag (write 0 to clear), 0-1h
3	Rd only	0h	FBO	FBO FIFO B Overflow Flag (write 0 to clear), 0-1h
2	Rd only	0h	FBU	FBU FIFO B Underflow Flag (write 0 to clear), 0-1h
1	Rd only	0h	FAO	FAO FIFO A Overflow Flag (write 0 to clear), 0-1h
0	Rd only	0h	FAU	FAU FIFO A Underflow Flag (write 0 to clear), 0-1h

4.3.4.4 SIUs_SIM: Sequencer Instruction Memory

I/O Address HIU_RDT

Index				
	2e00 (SIU0_SIM)	2e08 (SIU8_SIM)	2e10 (SIU16_SIM)	2e18 (SIU24_SIM)
	2e01 (SIU1_SIM)	2e09 (SIU9_SIM)	2e11 (SIU17_SIM)	2e19 (SIU25_SIM)
	2e02 (SIU2_SIM)	2e0a (SIU10_SIM)	2e12 (SIU18_SIM)	2e1a (SIU26_SIM)
	2e03 (SIU3_SIM)	2e0b (SIU11_SIM)	2e13 (SIU19_SIM)	2e1b (SIU27_SIM)
	2e04 (SIU4_SIM)	2e0c (SIU12_SIM)	2e14 (SIU20_SIM)	2e1c (SIU28_SIM)
	2e05 (SIU5_SIM)	2e0d (SIU13_SIM)	2e15 (SIU21_SIM)	2e1d (SIU29_SIM)
	2e06 (SIU6_SIM)	2e0e (SIU14_SIM)	2e16 (SIU22_SIM)	2e1e (SIU30_SIM)
	2e07 (SIU7_SIM)	2e0f (SIU15_SIM)	2e17 (SIU23_SIM)	2e1f (SIU31_SIM)

The 32 identical registers SIUs_SIM store the instruction sequence for fields 1 and 2

RSVD		OTN					EP	FA				OBA			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15 14	R/W	0h	RSVD	Reserved (read as 0)
13 9	R/W	0h	OTN	Offset to Next Instruction Specifies the signed, 5 bit displacement to the next instruction to execute (0-1f h)
8	R/W	0	EP	Exit Point Identifies the current instruction as the exit point when the field toggle condition is detected 0 Normal fall through instruction 1 Exit point instruction
7 4	R/W	0000	FA	FIFO Association Associates a FIFO with the current instruction 0000 FIFO G 0001 FIFO F 0010 FIFO E 0011 FIFO A 0100 FIFO B 0101 FIFO C 0110 FIFO D
3 0	R/W	0000	OBA	Object Buffer Association Associates an object buffer with the current instruction (see field FA) 0000 Object buffer 0 0001 Object buffer 1 0010 Object buffer 2 0011 Object buffer 3 0100 Object buffer 4 0101 Object buffer 5 0110 Object buffer 6 0111 Object buffer 7

4.3.5 ALU: Arithmetic and Logic Unit

4.3.5.1 ALU_MCR1: Master Control

I/O Address HIU_RDT
Index 2900 (ALU_MCR1 Master Control Field 1)
2901 (ALU_MCR2 Master Control Field 2)

See also ALU Arithmetic and Logic Unit, p. 63

Registers ALU_MCR1 and ALU_MCR2 specify the ALU operating mode for fields 1 and 2.

GRM	TF		AOP				VOUT		UOUT		VOUT		OPCS	OPBS	OPAS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	00	GRM	Three-operand Bit Mask selecting tag source 0 Bit per bit mask — one 16-bit value in FIFO C will mask one pixel in the ALU, tag bit per bit) 1 Bit per pixel mask — one 16-bit value in FIFO C will mask 16 pixels in the ALU (one tag bit per pixel)
14 13	R/W	0000	TF	Tag Format Specifies both the input and output stream format 00 No tag 01 Tagged 4 2 2 YCbCr data 10 Tagged 5 5 5 RGB data 11 Tagged 8 8 8 RGB data
12 9	R/W	00	AOP	Arithmetic Operation Select 0000 Alpha mix using alpha register (dA + (1 d)B) 0001 Alpha mix using operand C (cA + (1 c)B) 0010 Operand A + Operand B 0011 Operand A - Operand B 0100 (Operand A Operand B) / 2 0101 Reconstruct field from operands A and B 0110 Four frame interpolate from operands A and B 1000 Y scaling mode **** All other configurations are reserved, results of these configurations are unpredictable
8 7	R/W	00	YOUT	Y output Source Select 00 Source output from logical unit 01 Source output from arithmetic unit 10 Source output based on control tag 11 Enable arithmetic out based on tag
6 5	R/W	00	UOUT	U output Source Select 00 Source output from logical unit 01 Source output from arithmetic unit 10 Source output based on control tag 11 Enable arithmetic out based on tag
4 3	R/W	0	VOUT	V output Source Select 00 Source output from logical unit 01 Source output from arithmetic unit 10 Source output based on control tag 11 Enable arithmetic out based on tag
2	R/W	0	OPCS	Operand C Source Select 0 Operand sourced from constant register 1 Operand sourced from FIFO
1	R/W	0	OPBS	Operand B Source Select 0 Operand sourced from constant register 1 Operand sourced from FIFO
0	R/W	0	OPAS	Operand A Source Select 0 Operand sourced from constant register 1 Operand sourced from FIFO

4.3.5.2 ALU_TOP: Tag Operation

I/O Address HIU_RDT
Index 2902

See also Data Tagging, p. 66

Register ALU_TOP specifies the control and output tag multiplexer operation codes

CTC								OTC							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
15 8	R/W	0h	CTC	Control Tag Code (0-FFh)
7 0	R/W	0h	OTC	Output Tag Code (0 FFh)

4.3.5.3 ALU_AV: Alpha Value

I/O Address HIU_RDT
Index 2903

See also Arithmetic Operations, p. 67
Table 3-23 Arithmetic Operations, p. 67

Register ALU_AV specifies the alpha mix constant.

RSVD								AV							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:8	R/W	0h	RSVD	Reserved (read as 0)
7:0	R/W	0h	AV	Alpha Value (0:FFh)

4.3.5.4 ALU_LOPx: Logic Operation

I/O Address HIU_RDT
Index 2904 (ALU_LOPY, Logic Operation Channel Y)
2905 (ALU_LOPU, Logic Operation Channel U)
2906 (ALU_LOPV, Logic Operation Channel V)

See also Logical Operations, p. 67

Registers ALU_LOPY, ALU_LOPU, and ALU_LOPV specify the constant values for logical multiplexers A, B, and C, respectively.

MLOP															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:0	R/W	0h	MLOP	Multiplexor Logical Operation

4.3.5.5 ALU_CAx: Constant A

I/O Address HIU_RDT
Index 2907 (ALU_CAY, Constant A, Channel Y)
2908 (ALU_CAU, Constant A, Channel U)
2909 (ALU_CAV, Constant A, Channel V)

See also ALU_MCRI, Master Control, p. 128

Registers ALU_CAY, ALU_CAU, and ALU_CAV specify the constant values for Operand A, based on the value of field OPAS in register ALU_MCRI.

RSVD							TAG	CON							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:9	R/W	0h	RSVD	Reserved (read as 0)
8	R/W	0h	TAG	Tag. Specifies the constant tag bit to insert in the input stream. (0:1h)
7:0	R/W	0h	CON	Constant. Specifies the constant 8 bit value to use in place of the real time input stream channel for operand A. (0:FFh)

4.3.5.6 ALU_CBx: Constant B

I/O Address HIU_RDT
Index 290a (ALU_CBY, Constant B, Channel Y)
290b (ALU_CBU, Constant B, Channel U)
290c (ALU_CBV, Constant B, Channel V)

See also ALU_MCRI, Master Control, p. 128

Registers ALU_CBY, ALU_CBU, and ALU_CBV specify the constant values for Operand B, based on the value of field OPBS in register ALU_MCRI.

RSVD							TAG	CON							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:9	R/W	0h	RSVD	Reserved (read as 0)
8	R/W	0h	TAG	Tag. Specifies the constant tag bit to insert in the input stream. (0:1h)
7:0	R/W	0h	CON	Constant. Specifies the constant 8 bit value to use in place of the real time input stream channel for operand B. (0:FFh)

4.3.5.7 ALU_CCx: Constant C

I/O Address HIU_RDT
Index 290d (ALU_CCY Constant C, Channel Y)
290e (ALU_CCU Constant C, Channel U)
290f (ALU_CCV Constant C, Channel V)

See also ALU_MCRI Master Control, p. 128

Registers ALU_CCY, ALU_CCU, and ALU_CCV specify the constant values for Operand C, based on the value of field OPCS in register ALU_MCRI

RSVD							TAG	CON							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:9	R/W	0h	RSVD	Reserved (read as 0)
8	R/W	0h	TAG	Tag Specifies the constant tag bit to insert in the input stream (0-1h)
7:0	R/W	0h	CON	Constant Specifies the constant 8 bit value to use in place of the real-time input stream channel for operand C (0-FFh)

4.3.6 OPU: Output Processing Unit

4.3.6.1 OPU_MCRI: Master Control

I/O Address HIU_RDT
Index 2a00 (OPU_MCR1 Master Control Field 1)
2b00 (OPU_MCR2 Master Control Field 2)

See also Figure 3-24. OPU Output Processor Unit, p. 68

Registers OPU_MCR1 and OPU_MCR2 control the operation of the OPU for fields 1 and 2

FPS	IM	ZE	RSVD								IF			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	0	FPS	Field Polarity Select Controls the polarity of the field ID signal supplied to the Window Clipping subunit 0 Normal polarity 1 Invert polarity
14	R/W	0	IM	Interlace Mode Specifies the input stream as interlaced or non-interlaced data 0 Progressive scan input 1 Interlaced input
13	R/W	0	ZE	Zoom Enable Enables or disables the operation of the 2:1 X zoom subunit 0 Disable zoom 1 Enable 2 X zoom
12:4	R/W	0h	RSVD	Reserved (read as 0)
3:0	R/W	0000	IF	Input Data Format Specifies the format of the input data stream 0000 YCbCr 4:2:2 non-tagged data 0001 YCbCr 4:2:2 tagged data 1000 RGB 5:6:5 non-tagged data 1001 RGB 5:5:5 tagged data 1110 RGB 3:3:2 non-tagged data (non-zoom mode only)

4.3.6.2 OPU_XBI1: X Begin

I/O Address HIU_RDT
Index 2a02 (OPU_XBI1: X Begin Integer Field 1)
2b02 (OPU_XBI2: X Begin Integer Field 2)

See also Figure 3-24 OPU Output Processor Unit, p. 68

Registers OPU_XBI1 and OPU_XBI2 specify the 11 bit X begin value for fields 1 and 2.

RSVD					BI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15-11	R/W	0h	RSVD	Reserved (read as 0)
10-0	R/W	0h	BI	Begin X Column Integer Index: Specifies the 11 bit integer portion of the 11 bit X begin value (0-7FFh)

4.3.6.3 OPU_XEI1: X End

I/O Address HIU_RDT
Index 2a03 (OPU_XEI1: X End Integer Field 1)
2b03 (OPU_XEI2: X End Integer Field 2)

See also Figure 3-24 OPU Output Processor Unit, p. 68

Registers OPU_XEI1 and OPU_XEI2 specify the 11 bit X end value for fields 1 and 2

RSVD					EI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15-11	R/W	0h	RSVD	Reserved (read as 0)
10-0	R/W	0h	EI	End X Column Integer Index: Specifies the 11 bit X end value (0-7FFh)

4.3.6.4 OPU_YBI1: Y Begin

I/O Address HIU_RDT
Index 2a07 (OPU_YBI1: Y Begin Integer Field 1)
2b07 (OPU_YBI2: Y Begin Integer Field 2)

See also. Figure 3-24 OPU Output Processor Unit, p. 68

Registers OPU_YBI1 and OPU_YBI2 specify the 11 bit Y begin value for fields 1 and 2.

RSVD					BI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15-11	R/W	0h	RSVD	Reserved (read as 0)
10-0	R/W	0h	BI	Begin Y Row Integer Index: Specifies the 11 bit integer portion of the 11 bit Y begin value (0-7FFh)

4.3.6.5 OPU_YEI1: Y End

I/O Address HIU_RDT
Index 2a08 (OPU_YEI1: Y End Integer Field 1)
2b08 (OPU_YEI2: Y End Integer Field 2)

See also. Figure 3-24 OPU Output Processor Unit, p. 68

Registers OPU_YEI1 and OPU_YEI2 specify the 11 bit Y end value for fields 1 and 2

RSVD					EI										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15-11	R/W	0h	RSVD	Reserved (read as 0)
10-0	R/W	0h	EI	End Y Row Integer Index: Specifies the 11 bit Y end value (0-7FFh)

4.4 RFU: Reference Frame Unit — Registers

Table 4-6. RFU registers Accessed by the Register Data Port

Name	Index	Definition	Ref. Section
MMU: Memory Management Unit			
MMU_MCR	4000	Master Control	4.4.2.1, page 145
OBU: Object Buffer Unit			4.4.1, page 140
OBU0_MCR	4800	Object Buffer 0 Master Control	4.4.1.1, page 140
OBU0_RFX	4801	Object Buffer 0 Reference Frame X Size	4.4.1.2, page 141
OBU0_LSL	4802	Object Buffer 0 Linear Start Address Low	4.4.1.3, page 142
OBU0_LSH	4803	Object Buffer 0 Linear Start Address High	4.4.1.3, page 142
OBU0_BSX	4804	Object Buffer 0 Buffer X Size	4.4.1.4, page 143
OBU0_BSY	4805	Object Buffer 0 Buffer Y Size	4.4.1.4, page 143
OBU0_DEC	4806	Object Buffer 0 Decimate Control	4.4.1.5, page 144
OBU1_MCR	4810	Object Buffer 1 Master Control	4.4.1.1, page 140
OBU1_RFX	4811	Object Buffer 1 Reference Frame X Size	4.4.1.2, page 141
OBU1_LSL	4812	Object Buffer 1 Linear Start Address Low	4.4.1.3, page 142
OBU1_LSH	4813	Object Buffer 1 Linear Start Address High	4.4.1.3, page 142
OBU1_BSX	4814	Object Buffer 1 Buffer X Size	4.4.1.4, page 143
OBU1_BSY	4815	Object Buffer 1 Buffer Y Size	4.4.1.4, page 143
OBU1_DEC	4816	Object Buffer 1 Decimate Control	4.4.1.5, page 144
OBU2_MCR	4820	Object Buffer 2 Master Control	4.4.1.1, page 140
OBU2_RFX	4821	Object Buffer 2 Reference Frame X Size	4.4.1.2, page 141
OBU2_LSL	4822	Object Buffer 2 Linear Start Address Low	4.4.1.3, page 142
OBU2_LSH	4823	Object Buffer 2 Linear Start Address High	4.4.1.3, page 142
OBU2_BSX	4824	Object Buffer 2 Buffer X Size	4.4.1.4, page 143
OBU2_BSY	4825	Object Buffer 2 Buffer Y Size	4.4.1.4, page 143
OBU2_DEC	4826	Object Buffer 2 Decimate Control	4.4.1.5, page 144
OBU3_MCR	4830	Object Buffer 3 Master Control	4.4.1.1, page 140
OBU3_RFX	4831	Object Buffer 3 Reference Frame X Size	4.4.1.2, page 141
OBU3_LSL	4832	Object Buffer 3 Linear Start Address Low	4.4.1.3, page 142

Table 4-6. RFU registers Accessed by the Register Data Port *(cont.)*

Name	Index	Definition	Ref. Section
OBU3_LSH	4833	Object Buffer 3 Linear Start Address High	4.4.1.3, page 142
OBU3_BSX	4834	Object Buffer 3 Buffer X Size	4.4.1.4, page 143
OBU3_BSY	4835	Object Buffer 3 Buffer Y Size	4.4.1.4, page 143
OBU3_DEC	4836	Object Buffer 3 Decimate Control	4.4.1.5, page 144
OBU4_MCR	4840	Object Buffer 4 Master Control	4.4.1.1, page 140
OBU4_RFX	4841	Object Buffer 4 Reference Frame X Size	4.4.1.2, page 141
OBU4_LSL	4842	Object Buffer 4 Linear Start Address Low	4.4.1.3, page 142
OBU4_LSH	4843	Object Buffer 4 Linear Start Address High	4.4.1.3, page 142
OBU4_BSX	4844	Object Buffer 4 Buffer X Size	4.4.1.4, page 143
OBU4_BSY	4845	Object Buffer 4 Buffer Y Size	4.4.1.4, page 143
OBU4_DEC	4846	Object Buffer 4 Decimate Control	4.4.1.5, page 144
OBU5_MCR	4850	Object Buffer 5 Master Control	4.4.1.1, page 140
OBU5_RFX	4851	Object Buffer 5 Reference Frame X Size	4.4.1.2, page 141
OBU5_LSL	4852	Object Buffer 5 Linear Start Address Low	4.4.1.3, page 142
OBU5_LSH	4853	Object Buffer 5 Linear Start Address High	4.4.1.3, page 142
OBU5_BSX	4854	Object Buffer 5 Buffer X Size	4.4.1.4, page 143
OBU5_BSY	4855	Object Buffer 5 Buffer Y Size	4.4.1.4, page 143
OBU5_DEC	4856	Object Buffer 5 Decimate Control	4.4.1.5, page 144
OBU6_MCR	4860	Object Buffer 6 Master Control	4.4.1.1, page 140
OBU6_RFX	4861	Object Buffer 6 Reference Frame X Size	4.4.1.2, page 141
OBU6_LSL	4862	Object Buffer 6 Linear Start Address Low	4.4.1.3, page 142
OBU6_LSH	4863	Object Buffer 6 Linear Start Address High	4.4.1.3 page 142
OBU6_BSX	4864	Object Buffer 6 Buffer X Size	4.4.1.4, page 143
OBU6_BSY	4865	Object Buffer 6 Buffer Y Size	4.4.1.4, page 143
OBU6_DEC	4866	Object Buffer 6 Decimate Control	4.4.1.5, page 144
OBU7_MCR	4870	Object Buffer 7 Master Control	4.4.1.1, page 140
OBU7_RFX	4871	Object Buffer 7 Reference Frame X Size	4.4.1.2 page 141
OBU7_LSL	4872	Object Buffer 7 Linear Start Address Low	4.4.1.3, page 142
OBU7_LSH	4873	Object Buffer 7 Linear Start Address High	4.4.1.3 page 142

Table 4-6. RFU registers Accessed by the Register Data Port *(cont.)*

Name	Index	Definition	Ref. Section
OBJ7_BSX	4874	Object Buffer 7 Buffer X Size	4.4.1.4, page 143
OBJ7_BSY	4875	Object Buffer 7 Buffer Y Size	4.4.1.4, page 143
OBJ7_DEC	4876	Object Buffer 7 Decimate Control	4.4.1.5, page 144
DWU: Display Window Unit			4.4.3, page 146
DWU_MCR	4100	Display Window Master Control	4.4.3.1, page 146
DWU_HCR	4101	Display Window Horizontal Control Register	4.4.3.2, page 147
DWU0_DZF	4400	Display Window 0 Display Zoom Factor	4.4.3.3, page 148
DWU0_RFX	4401	Display Window 0 Reference Frame X Size	4.4.3.4, page 149
DWU0_LSL	4402	Display Window 0 Linear Start Address Low	4.4.3.5, page 150
DWU0_LSH	4403	Display Window 0 Linear Start Address High	4.4.3.5, page 150
DWU0_WSX	4404	Display Window 0 Window X Size	4.4.3.6, page 151
DWU0_WSY	4405	Display Window 0 Window Y Size	4.4.3.6, page 151
DWU0_DSX	4406	Display Window 0 Display X Start	4.4.3.7, page 152
DWU0_DSY	4407	Display Window 0 Display Y Start	4.4.3.7, page 152
DWU1_DZF	4410	Display Window 1 Display Zoom Factor	4.4.3.3, page 148
DWU1_RFX	4411	Display Window 1 Reference Frame X Size	4.4.3.4, page 149
DWU1_LSL	4412	Display Window 1 Linear Start Address Low	4.4.3.5, page 150
DWU1_LSH	4413	Display Window 1 Linear Start Address High	4.4.3.5, page 150
DWU1_WSX	4414	Display Window 1 Window X Size	4.4.3.6, page 151
DWU1_WSY	4415	Display Window 1 Window Y Size	4.4.3.6, page 151
DWU1_DSX	4416	Display Window 1 Display X Start	4.4.3.7, page 152
DWU1_DSY	4417	Display Window 1 Display Y Start	4.4.3.7, page 152
DWU2_DZF	4420	Display Window 2 Display Zoom Factor	4.4.3.3, page 148
DWU2_RFX	4421	Display Window 2 Reference Frame X Size	4.4.3.4, page 149
DWU2_LSL	4422	Display Window 2 Linear Start Address Low	4.4.3.5, page 150
DWU2_LSH	4423	Display Window 2 Linear Start Address High	4.4.3.5, page 150
DWU2_WSX	4424	Display Window 2 Window X Size	4.4.3.6, page 151
DWU2_WSY	4425	Display Window 2 Window Y Size	4.4.3.6, page 151

Table 4-6. RFU registers Accessed by the Register Data Port *(cont.)*

Name	Index	Definition	Ref. Section
DWU2_DSX	4426	Display Window 2 Display X Start	4.4.3.7, page 152
DWU2_DSY	4427	Display Window 2 Display Y Start	4.4.3.7, page 152
DWU3_DZF	4430	Display Window 3 Display Zoom Factor	4.4.3.3, page 148
DWU3_RFX	4431	Display Window 3 Reference Frame X Size	4.4.3.4, page 149
DWU3_LSL	4432	Display Window 3 Linear Start Address Low	4.4.3.5, page 150
DWU3_LSH	4433	Display Window 3 Linear Start Address High	4.4.3.5, page 150
DWU3_WSX	4434	Display Window 3 Window X Size	4.4.3.6, page 151
DWU3_WSY	4435	Display Window 3 Window Y Size	4.4.3.6, page 151
DWU3_DSX	4436	Display Window 3 Display X Start	4.4.3.7, page 152
DWU3_DSY	4437	Display Window 3 Display Y Start	4.4.3.7, page 152

4.4.1 OBU: Object Buffer Unit

4.4.1.1 OBUo_MCR: Object Buffer Master Control

I/O Address Index — HIU_RDT
4800 (OBU0_MCR: Object Buffer 0 Master Control)
4810 (OBU1_MCR: Object Buffer 1 Master Control)
4820 (OBU2_MCR: Object Buffer 2 Master Control)
4830 (OBU3_MCR: Object Buffer 3 Master Control)
4840 (OBU4_MCR: Object Buffer 4 Master Control)
4850 (OBU5_MCR: Object Buffer 5 Master Control)
4860 (OBU6_MCR: Object Buffer 6 Master Control)
4870 (OBU7_MCR: Object Buffer 7 Master Control)

See also — Figure 3-28. Object Buffer, p. 72
Figure 3-29. XY BLT Direction Control, p. 75

The eight identical registers OBUo_MCR control the operation of the eight object buffers.

RSVD			LME	CME	OPM					SSM	YBDC	XBDC	FA		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description
15:13	R/W	000	RSVD — Reserved (read as 0)
12	R/W	0	LME — Luminance Mask Enable. Specifies whether the MSB of a 16 bit input stream (typically the Y channel of YCbCr data) is written to the object buffer or masked 0 Enable luminance data update 1 Disable luminance data update
11	R/W	0	CME — Chrominance Mask Enable. Specifies whether the LSB of a 16 bit input stream (typically the CbCr channel of YCbCr data) is written to the object buffer or masked 0 Enable chrominance data update 1 Disable chrominance data update
10:6	R/W	0h	OPM — Operation Mode. Enables or disables operation of the object buffer and specifies the synchronization and addressing modes 00000 Disable OBU 00001 Enable OBU, lock to IPU1, address generation locked to IPU1 00100 Enable OBU, independent, interlaced addresses, start on line 1 00101 Enable OBU, independent, interlaced addresses, start on line 2 01100 Enable OBU, independent, normal addresses 01101 Enable OBU, independent, line replicate addresses (on read) 01110 Enable OBU, independent, block mode addresses (8x8 blocks, OBU0 only) 01111 Enable 16x8 blocks, OBU0 only xxxxx All other configurations reserved, to ensure future compatibility, do not use

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Bit #	Access	Reset	Description (cont.)
5	R/W	0	SSM — Single Sweep Mode 0 Disable single sweep mode 1 Enable single sweep mode (reset OPM to 00000 after one blit)
4	R/W	0	YBDC — Y BLT Direction Control. Specifies whether the Y address counter is incremented or decremented after each line (see Figure 3-22) 0 BLT to decreasing memory addresses 1 BLT to increasing memory addresses
3	R/W	0	XBDC — X BLT Direction Control. Specifies whether the X address counter is incremented or decremented after each line (see Figure 3-22) 0 BLT to decreasing memory addresses 1 BLT to increasing memory addresses
2:0	R/W	000	FA — FIFO Association. Specifies whether the stream written into the object buffer is to be copied to one of the output FIFOs 000 No FIFO copy 001 Copy object buffer to FIFO A during write 010 Copy object buffer to FIFO B during write 011 Copy object buffer to FIFO C during write 100 Copy object buffer to FIFO D during write

4.4.1.2 OBUo_RFX: Object Buffer Reference Frame X Size

I/O Address Index — HIU_RDT
4801 (OBU0_RFX: Object Buffer 0 Reference Frame X Size)
4811 (OBU1_RFX: Object Buffer 1 Reference Frame X Size)
4821 (OBU2_RFX: Object Buffer 2 Reference Frame X Size)
4831 (OBU3_RFX: Object Buffer 3 Reference Frame X Size)
4841 (OBU4_RFX: Object Buffer 4 Reference Frame X Size)
4851 (OBU5_RFX: Object Buffer 5 Reference Frame X Size)
4861 (OBU6_RFX: Object Buffer 6 Reference Frame X Size)
4871 (OBU7_RFX: Object Buffer 7 Reference Frame X Size)

See also — Figure 3-28. Object Buffer, p. 72

The eight identical registers OBUo_RFX specify, for each of the eight object buffers, the 11 bit width (in pixels) of the reference frame containing the object buffer.

RSVD					RFX										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description
15:11	R/W	0h	RSVD — Reserved (read as 0)
10:0	R/W	0h	RFX — Reference Frame X size (0 /1 FFh)

4.4.1.3 OBUo_LSb: Object Buffer Linear Start Address

I/O Address HIU_RDT
Index
4802 (OBUo_LSL Object Buffer 0 Linear Start Address Low)
4812 (OBU1_LSL Object Buffer 1 Linear Start Address Low)
4822 (OBU2_LSL Object Buffer 2 Linear Start Address Low)
4832 (OBU3_LSL Object Buffer 3 Linear Start Address Low)
4842 (OBU4_LSL Object Buffer 4 Linear Start Address Low)
4852 (OBU5_LSL Object Buffer 5 Linear Start Address Low)
4862 (OBU6_LSL Object Buffer 6 Linear Start Address Low)
4872 (OBU7_LSL Object Buffer 7 Linear Start Address Low)

4803 (OBUo_LSH Object Buffer 0 Linear Start Address High)
4813 (OBU1_LSH Object Buffer 1 Linear Start Address High)
4823 (OBU2_LSH Object Buffer 2 Linear Start Address High)
4833 (OBU3_LSH Object Buffer 3 Linear Start Address High)
4843 (OBU4_LSH Object Buffer 4 Linear Start Address High)
4853 (OBU5_LSH Object Buffer 5 Linear Start Address High)
4863 (OBU6_LSH Object Buffer 6 Linear Start Address High)
4873 (OBU7_LSH Object Buffer 7 Linear Start Address High)

See also Figure 3-28 Object Buffer, p. 72

Registers OBUo_LSL and OBUo_LSH specify the 23 bit linear starting address of the object buffer.

Object Buffer Linear Start Address Low

Bits 15 through 0 of register OBUo_LSL specify the lower 16 bits of the 23 bit linear address.

LSL															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:1	R/W	0h	LSL	Linear Start Address Low. Specifies the lower bits of the 23 bit linear starting address (0-7FFFh)
0	R/W	0	LSB	Linear Start Address (LSB must = 0)

Object Buffer Linear Start Address High

Bits 5 through 0 of register OBUo_LSH specify the upper 6 bits of the 22 bit linear address.

RSVD										LSH					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:7	R/W	0h	RSVD	Reserved (read as 0)
6:0	R/W	0h	RSVD	Linear Start Address High. Specifies the upper 7 bits of the 23-bit linear starting address (0-7Fh)

4.4.1.4 OBUo_BSa: Object Buffer Size

I/O Address HIU_RDT
Index
4804 (OBUo_BSX Object Buffer 0 Buffer X Size)
4814 (OBU1_BSX Object Buffer 1 Buffer X Size)
4824 (OBU2_BSX Object Buffer 2 Buffer X Size)
4834 (OBU3_BSX Object Buffer 3 Buffer X Size)
4844 (OBU4_BSX. Object Buffer 4 Buffer X Size)
4854 (OBU5_BSX Object Buffer 5 Buffer X Size)
4864 (OBU6_BSX Object Buffer 6 Buffer X Size)
4874 (OBU7_BSX. Object Buffer 7 Buffer X Size)

4805 (OBUo_BSY Object Buffer 0 Buffer Y Size)
4815 (OBU1_BSY Object Buffer 1 Buffer Y Size)
4825 (OBU2_BSY Object Buffer 2 Buffer Y Size)
4835 (OBU3_BSY Object Buffer 3 Buffer Y Size)
4845 (OBU4_BSY. Object Buffer 4 Buffer Y Size)
4855 (OBU5_BSY Object Buffer 5 Buffer Y Size)
4865 (OBU6_BSY Object Buffer 6 Buffer Y Size)
4875 (OBU7_BSY Object Buffer 7 Buffer Y Size)

See also Figure 3-28 Object Buffer, p. 72

Registers OBUo_BSX and OBUo_BSY specify the size of the object buffer.

Object Buffer X Size

The X size of the Object Buffer is its width in pixels. The hardware always forces the LSB to 0.

RSVD					BSX										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	BSX	Buffer X Size (0-7FFh)

Object Buffer Y Size

The Y size of the Object Buffer is its height in pixels.

RSVD					BSY										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	BSY	Buffer Y Size (0-7FFh)

4.4.1.5 OBUo_DEC: Object Buffer Decimate Control

I/O Address HIU_RDT
Index 4806 (OBU0_DEC: Object Buffer 0 Decimate Control)
4816 (OBU1_DEC: Object Buffer 1 Decimate Control)
4826 (OBU2_DEC: Object Buffer 2 Decimate Control)
4836 (OBU3_DEC: Object Buffer 3 Decimate Control)
4846 (OBU4_DEC: Object Buffer 4 Decimate Control)
4856 (OBU5_DEC: Object Buffer 5 Decimate Control)
4866 (OBU6_DEC: Object Buffer 6 Decimate Control)
4876 (OBU7_DEC: Object Buffer 7 Decimate Control)

Register OBUo_DEC specifies the write decimation mask. Fields DM7-DM0 are mapped to each successive group of eight pixels written into the object buffer. If a bit = 0, its corresponding pixel is written; if a bit = 1, its corresponding pixel is dropped

RSVD								DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description
15:8	R/W	0h	RSVD Reserved (read as 0)
7	R/W	0h	DM7 Write Decimation Mask Bit 7 0 Write pixel to Frame Buffer 1 Drop pixel
6	R/W	0h	DM6 Write Decimation Mask Bit 6 0 Write pixel to Frame Buffer 1 Drop pixel
5	R/W	0h	DM5 Write Decimation Mask Bit 5 0 Write pixel to Frame Buffer 1 Drop pixel
4	R/W	0h	DM4 Write Decimation Mask Bit 4 0 Write pixel to Frame Buffer 1 Drop pixel
3	R/W	0h	DM3 Write Decimation Mask Bit 3 0 Write pixel to Frame Buffer 1 Drop pixel
2	R/W	0h	DM2 Write Decimation Mask Bit 2 0 Write pixel to Frame Buffer 1 Drop pixel
1	R/W	0h	DM1 Write Decimation Mask Bit 1 0 Write pixel to Frame Buffer 1 Drop pixel

Bit #	Access	Reset	Description (cont.)
0	R/W	0h	DM0 Write Decimation Mask Bit 0 0 Write pixel to Frame Buffer 1 Drop pixel

4.4.2 MMU: Memory Management Unit

4.4.2.1 MMU_MCR: Master Control

I/O Address HIU_RDT
Index 4000

Register MMU_MCR specifies the characteristics of the Frame Buffer used by the CL-PX2070

RSVD											FBD	FBC			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description
15:5	R/W	0h	RSVD Reserved (read as 0)
4	R/W	0	FBD Frame Buffer Data Bus Width 0 16 bit wide bus 1 32 bit wide bus
3:0	R/W	0000	FBC Frame Buffer Address Configuration 0000 64K 0001 128K 0010 256K 0011 1 M

4.4.3 DWU: Display Window Unit

4.4.3.1 *DWU_MCR: Display Window Master Control*

I/O Address HIU_RDT
Index 4100 (DWU_MCR: Display Window Master Control)

See also Figure 3-30 Display Window, p. 77

Register DWU_MCR controls the operation of the display window and indicates to the RFU whether or not the CL-PX2080 is present.

GCS	GFP	GFM	GVSP	GHSP	GBP	OCC	IMS	RSVD				WC3	WC2	WC1	WC0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15	R/W	0	GCS	Graphics Clock Select 0 1/2x GPCLK 1 1x GPCLK
14	R/W	0	GFP	Graphics Field Polarity 0 normal polarity 1 inverted polarity
13	R/W	0	IMS	Graphics Field Mode 0 field polarity determined by value of GHSP on falling GVSP 1 GHSP input used as field select
12	R/W	0	GVSP	Graphics Vsync Polarity 0 active low 1 active high
11	R/W	0	GHSP	Graphics Hsync Polarity 0 active low 1 active high
10	R/W	0	GBP	Graphics Blank Polarity 0 active low 1 active high
9	R/W	0	OCC	Occluded Window Control. Specifies whether the present hardware configuration includes the CL-PX2080 0 CL-PX2080 is present — system supports occluded windows 1 CL-PX2080 is not present — system does not support occluded windows
8	R/W	0	GFM	Interlace Mode Select. Specifies whether the stream stored in the object buffer for display by the current display window is interlaced or non-interlaced 0 Progressive video (non-interlaced) 1 Interlaced video
7-4	R/W	0000	GVSP	Reserved (read as 0)

Bit #	Access	Reset	Description (cont.)	
3	R/W	0	WC3	Window 3 Control 0 Disable window 1 Enable window
2	R/W	0	WC2	Window 2 Control 0 Disable window 1 Enable window
1	R/W	0	WC1	Window 1 Control 0 Disable window 1 Enable window
0	R/W	0	WC0	Window 0 Control 0 Disable window 1 Enable window

4.4.3.2 *DWU_HCR: Display Window Horizontal Control Register*

I/O Address HIU_RDT
Index 4101 (DWU_HCR: Display Window Horizontal Control Register)

See also Figure 3-30 Display Window, p. 77
DWU Display Window Unit, p. 76

Register DWU_HCR shares two functions, depending on whether or not the CL-PX2070 is operating with the CL-PX2080, as specified by Bit OCC of register DWU_MCR.

Horizontal Active Count

When Bit OCC of register DWU_MCR = 0, the CL-PX2070 is operating with the CL-PX2080, and DWU_MCR specifies the number of pixel periods in the horizontal line active interval for the output CRT display.

RSVD					HAC										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	HAC	Horizontal Active Count (0-7FFh)

Minimum Window Separation

When Bit OCC of register DWU_MCH = 1, the CL-PX2070 is not operating with the CL-PX2080, and DWU_HCR specifies the minimum number of pixel periods required to separate display windows.

RSVD								MWS							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:8	R/W	0h	RSVD	Reserved (read as 0)
7:0	R/W	0h	MWS	Minimum Window Separation (0:FFh)

4.4.3.3 DWUd_DZF: Display Window Display Zoom Factor

I/O Address HIU_RDT
Index 4400 (DWU0_DZF: Display Window 0 Display Zoom Factor)
4410 (DWU1_DZF: Display Window 1 Display Zoom Factor)
4420 (DWU2_DZF: Display Window 2 Display Zoom Factor)
4430 (DWU3_DZF: Display Window 3 Display Zoom Factor)

Register DWUd_DZF specifies the X and Y zoom factors to be applied to the display window output. Functional only when used with CL-PX2080. Specifies zoom factor. The image is scaled according to the following formula:

$$\text{Scaling} = \frac{256}{\text{ZOOM FACTOR}}$$

For example, a zoom factor of 128 yields a scaling factor of 2. A scaling factor of one (no change in image size) is selected by entering a zoom factor of zero.

NOTE: The contents of the object buffer are not affected by the zoom factors.

YZOOM								XZOOM							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:8	R/W	0h	YZOOM	Y Zoom Factor — line replication value (0:FFh)
7:0	R/W	0h	XZOOM	X Zoom Factor — pixel replication value (0:FFh)

4.4.3.4 DWUd_RFX: Display Window Reference Frame X Size

I/O Address HIU_RDT
Index 4401 (DWU0_RFX: Display Window 0 Reference Frame X Size)
4411 (DWU1_RFX: Display Window 1 Reference Frame X Size)
4421 (DWU2_RFX: Display Window 2 Reference Frame X Size)
4431 (DWU3_RFX: Display Window 3 Reference Frame X Size)

See also Figure 3.30 Display Window, p. 77

Register DWUd_RFX specifies the 11 bit pixel width of the reference frame containing the display window.

RSVD					RFX										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	RFX	Reference Frame X size (0:7FFh)

4.4.3.5 DWUd_LSb: Display Window Linear Start Address

I/O Address Index — HIU_RDT

4402 (DWU0_LSL Display Window 0 Linear Start Address Low)
4412 (DWU1_LSL Display Window 1 Linear Start Address Low)
4422 (DWU2_LSL Display Window 2 Linear Start Address Low)
4432 (DWU3_LSL Display Window 3 Linear Start Address Low)

4403 (DWU0_LSH Display Window 0 Linear Start Address High)
4413 (DWU1_LSH Display Window 1 Linear Start Address High)
4423 (DWU2_LSH Display Window 2 Linear Start Address High)
4433 (DWU3_LSH Display Window 3 Linear Start Address High)

See also — Figure 3-30 Display Window, p. 77

Register DWUd_LSL and DWUd_LSH specify the 23 bit linear starting address of the display window.

Display Window Linear Start Address Low

Bits 15 through 0 of register DWUd_LSL specify the lower 16 bits of the 23-bit linear address.

LSL															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:1	R/W	0h	LSL	Linear Start Address Low. Specifies the lower bits of the 23 bit linear starting address (0-7FFFh)
0	R/W	0	LSB	Linear Start Address (LSb must = 0)

Display Window Linear Start Address High

Bits 6 through 0 of register DWUd_LSH specify the upper 7 bits of the 23 bit linear address.

RSVD									LSH						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:7	R/W	0h	RSVD	Reserved (read as 0)
6:0	R/W	0h	LSH	Linear Start Address High. Specifies the upper 7 bits of the 23-bit linear starting address (0-7Fh)

4.4.3.6 DWUd_WSe: Display Window Size

I/O Address Index — HIU_RDT

4404 (DWU0_WSX Display Window 0 Window X Size)
4414 (DWU1_WSX Display Window 1 Window X Size)
4424 (DWU2_WSX Display Window 2 Window X Size)
4434 (DWU3_WSX Display Window 3 Window X Size)

4405 (DWU0_WSY Display Window 0 Window Y Size)
4415 (DWU1_WSY Display Window 1 Window Y Size)
4425 (DWU2_WSY Display Window 2 Window Y Size)
4435 (DWU3_WSY Display Window 3 Window Y Size)

See also — Figure 3-30 Display Window, p. 77

Registers DWUd_WSX and DWUd_WSY specify the size of the display window.

Display Window X Size

Register DWUd_WSX specifies the X dimension of the display window in pixels

RSVD					WSX										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	WSX	Window X Size (LSb must = 0)

Display Window Y Size

Register DWUd_WSY specifies the Y dimension of the display window in pixels

RSVD					WSY										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:11	R/W	0h	RSVD	Reserved (read as 0)
10:0	R/W	0h	WSY	Window Y Size (0-7FFh)

4.4.3.7 DWUd_DSa: Display Window Display Start

I/O Address: HIU RDT

Index:
- 4406 (DWU0 DSX Display Window 0 Display X Start)
- 4416 (DWU1 DSX Display Window 1 Display X Start)
- 4426 (DWU2 DSX Display Window 2 Display X Start)
- 4436 (DWU3 DSX Display Window 3 Display X Start)
- 4407 (DWU0 DSY Display Window 0 Display Y Start)
- 4417 (DWU1 DSY Display Window 1 Display Y Start)
- 4427 (DWU2 DSY Display Window 2 Display Y Start)
- 4437 (DWU3 DSY Display Window 3 Display Y Start)

See also: Figure 3-30 Display Window, p. 77

Registers DWUd DSX and DWUd DSY specify the location of the top left corner of the display window relative to the top left corner of the output CRT display.

Display Window Display X Start

Register DWUd DSX specifies the pixel offset from the CRT column 0 to the left most column of the display window

RSVD				DSX											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:12	R/W	0h	RSVD	Reserved (read as 0)
11:0	R/W	0h	DSX	Display X Start (0-7FFh)

Display Window Display Y Start

Register DWUd DSY specifies the pixel offset from the CRT row 0 to the top-most row of the display window

RSVD				DSY											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
15:12	R/W	0h	RSVD	Reserved (read as 0)
11:0	R/W	0h	DSY	Display Y Start (0-7FFh)

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

This section lists the absolute maximum ratings of the CL-PX2070. Stresses above those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Storage temperature	-65° to +150° C
Voltage on any pin with respect to ground	-0.5 Volts to V_{DD} +0.5V
Power Supply Voltage	7V
Lead Temperature (10 seconds)	300° C

5.2 CL-PX2070 Specifications (Digital)

Symbol	Parameter	MIN	MAX	Units	Conditions
VDD	Power Supply Voltage	4.75	5.25	V	Normal Operation
V_{IL}	Input Low Voltage	0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{DD} + 0.8	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 µA
I_{DD}	Digital Supply Current		N/A	mA	V_{DD} Nominal
I_{DDT}	Total Supply Current		N/A	mA	Note 1
I_L	Input Leakage	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

NOTE: 1) I_{DDT} is the sum of I_{DD} + $DACI_{DD}$ + $CLKI_{DD}$, and must be <200 mA (package constraint)
2) DACVSS must not exceed V_{DD}.

5.3 CL-PX2070 DC Characteristics

(VDD = 5V 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
I_{Omax}	Output Current		2.1	mA	V_O < 1 V
Co	Output Capacitance		12	pf	Blanke = V_{IL} MAX

NOTE: 1) t_D is measured from the 50% point of VDCLK to 50% point of full scale transition
2) Load is 37.5 ohms and 30 pF per analog output
3) I_{REF} = 8.8 mA
4) t_R is measured from 10% to 90% full scale.
5) t_S is measured from 50% point of full scale transition to output remaining within 2% of final value.
6) Outputs loaded identically
7) About the mid point of the distribution of the three DACs measured at full scale deflection

5.4 AC Characteristics/Timing Information

This section includes system timing requirements for the CL-PX2080. Timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0 to 70° C, and V_{CC} varying from 4.75 to 5.25V DC.

NOTE: 1 All timings assume a load of 50 pF
2 TTL signals are measured at TTL threshold, CMOS signals are measured at CMOS threshold

5.4.1 Index of Timing Information

5.4.2 I/O Timing (ISA Bus)

Table 5-1. I/O Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_1	Setup time, valid address to IOR*/IOW* active	30		ns
t_2	Delay, IOR*/IOW* active to DEN* active, DDIR change	4	20	ns
t_3	Delay, IOR* active to data out low Z	4	75	ns
t_4	Delay, IOR* active to data out valid		75	ns
t_5	Pulse width, IOR*/IOW*	100		ns
t_6	Delay, IOR*/IOW* inactive to DEN* inactive, DDIR change	4	20	ns
t_7	IOR* inactive to Three-State delay	4	20	ns
t_8	Address hold time from IOR*/IOW* active	0		ns
t_9	Setup time, data valid to IOW* inactive	50		ns
t_{10}	Hold time, IOW* inactive to data invalid	0		ns
t_{11}	Delay, IOW* inactive to next IOW* or IOR* active	80		ns
t_{12}	Setup, AEN rising edge to IOW* or IOR* active	20		ns
t_{13}	Delay, IOW* or IOR* inactive to AEN falling edge	0		ns

NOTE: AEN must be low

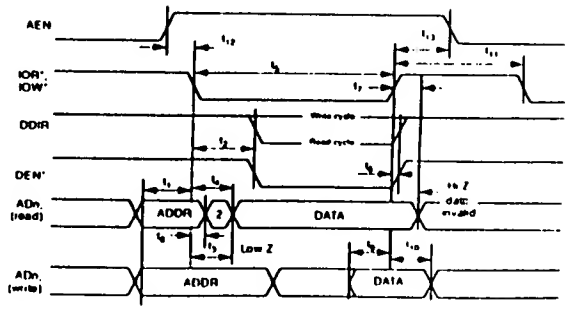


Figure 5-1. I/O Timing (ISA Bus)

5.4.3 DMA Timing (ISA Bus)

Table 5-2. DMA Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_1	Delay, IOR*/IOW* active to DEN* active, DDIR change	4	20	ns
t_2	Delay, IOR* active to data out low Z	4	75	ns
t_3	Delay, IOR* active to data out valid		75	ns
t_4	Pulse width, IOR*/IOW*	100		ns
t_5	Delay, IOR*/IOW* inactive to DEN* inactive, DDIR change	4	20	ns
t_6	IOR* inactive to Three State delay	4	20	ns
t_7	Setup time, data valid to IOW* inactive	50		ns
t_8	Hold time, IOW* inactive to data invalid	0		ns
t_9	Delay, IOW* inactive to next IOW* or IOR* active	80		ns
t_{10}	Delay, BCLK rising edge to DMARQ inactive			ns

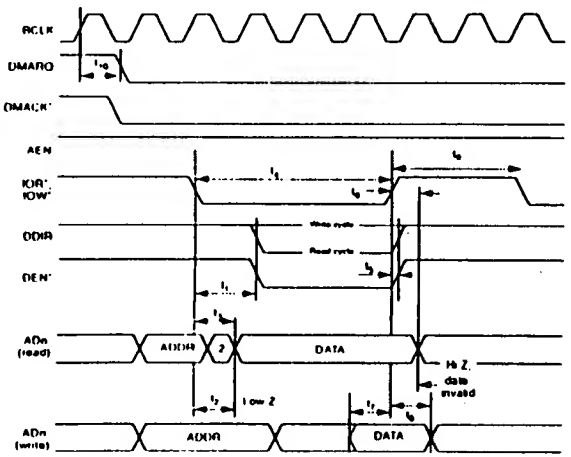


Figure 5-2. DMA Timing (ISA Bus)

5.4.4 MCA I/O Cycle Timing

Table 5-3. MCA I/O Cycle Timing

Symbol	Parameter	MIN	MAX	Unit
t_1	Setup time, address valid to ADL* active	40		ns
t_2	Setup time, status valid to ADL* active	7		ns
t_3	Pulse width, ADL*	35		ns
t_4	Hold time, status from ADL* inactive	20		ns
t_5	Hold time, address, MI/O* from ADL* inactive	25		ns
t_6	Setup time, address valid to CMD* active	80		ns
t_7	Setup time, status valid to CMD* active	50		ns
t_8	Setup time, ADL* active to CMD* active	35		ns
t_9	Pulse width, CMD*	90		ns
t_{10}	Hold time, address, from CMD* active	25		ns
t_{11}	Hold time, status, from CMD* active	25		ns
t_{12}	Setup time, write data valid to CMD* active	15		ns
t_{13}	Hold time, write data valid from CMD* active	0		ns
t_{14}	Delay, CMD* active to read data valid	45		ns
t_{15}	Delay, CMD* inactive to read data invalid	0		ns
t_{16}	Delay, CMD* inactive to read data high Z		30	ns
t_{17}	Delay, CMD* active to DEN* active / DDIR change		35	ns
t_{18}	Delay, CMD* inactive to DEN* inactive / DDIR change		20	ns
t_{19}	Delay, CMD* inactive to CMD* active			ns

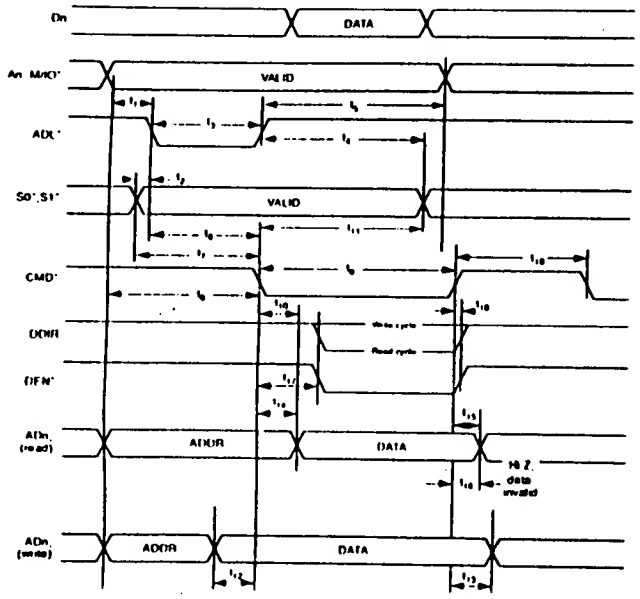


Figure 5-3. MCA I/O Cycle Timing

5.4.5 CDSFDBK* Timing (MCA Bus)

Table 5-4. CDSFDBK* Timing (MCA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_1	Address, M/IO* valid to CDSFDBK delay		55	ns
t_2	Address, M/IO*, invalid, CDSFDBK inactive	0		ns

NOTE: Slaves do not drive CD_S_FDBK* when they are selected by the 'card setup' signal

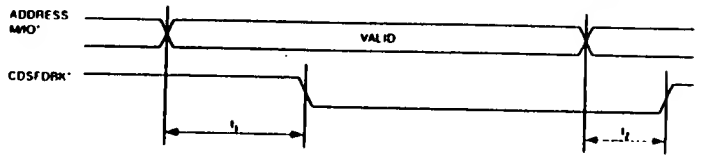


Figure 5-4. CDSFDBK* Timing (MCA Bus)

5.4.6 CDSETUP* Timing (MCA Bus)

Table 5-5. CDSETUP* Timing (MCA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_1	CD_SETUP* active setup to ADL* active	10		ns
t_2	CMD* active to CD_SETUP* inactive hold	25		ns
t_3	ADL* inactive to CD_SETUP* inactive hold	20		ns

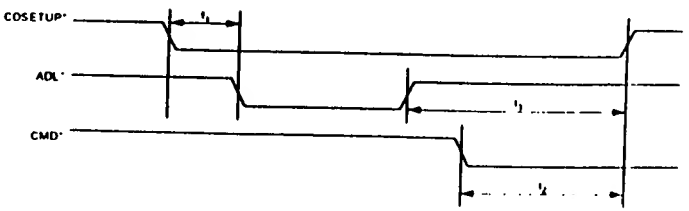


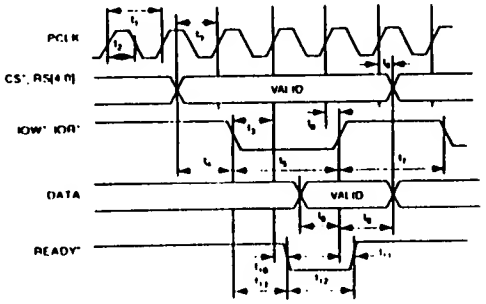
Figure 5-5. CDSETUP* Timing (MCA Bus)

5.4.7 Write Timing (Local Hardware Interface)

Table 5-6. Local Hardware Interface Mode Write

Symbol	Parameter	MIN	MAX	Unit
t_1	period, PCLK	30		ns
t_2	pulse width, PCLK	12		ns
t_3	setup time, IOW*, CS* to PCLK rising edge	10		ns
t_4	setup time, CS*, RS[4:0] to IOW*	1		cycle
t_5	pulse width, IOW*	2		cycle
t_6	hold time, PCLK rising edge to IOW*, CS*	2		ns
t_7	delay, IOW* inactive to IOW* or IOR* active	2		cycles
t_8	setup time, DATA valid to IOW* inactive	15		ns
t_9	hold time, CS*, RS[4:0], DATA valid to IOW* inactive	2		ns
t_{10}	delay, PCLK rising edge to READY* active	4	20	ns
t_{11}	delay, IOW* inactive to READY* inactive	4	20	ns
t_{12}	pulse width, READY*	1	2	cycles
t_{13}	delay, IOW* active to READY* active	1	1	cycle

NOTE: 1) CS*, IOW*, RS[4:0] must be asserted
2) If IOW* exceeds 2 cycles, READY* is negated after 2 cycles. In this case, t_{11} is referenced to CLK.



NOTE:

Timing is shown relative to clock. Internally, Data, R*/W, RS[3:1] must be stable entire cycle following CS* active. Data is written on 2nd rising edge after CS* is asserted

Figure 5-6. Write Timing (Local Hardware Interface)

5.4.8 Read Timing (Local Hardware Interface)

Table 5-7. Local Hardware Interface Mode Read

Symbol	Parameter	MIN	MAX	Unit
t_1	period, PCLK	30		ns
t_2	pulse width, PCLK	12		ns
t_3	setup time, IOR*, CS* active to CLK rising edge	12		ns
t_4	setup time, CS*, RS[4:0] valid to IOR* active	1		cycle
t_5	pulse width, IOR*	3		cycles
t_6	hold time, PCLK rising edge to IOR* inactive, CS* inactive	2		ns
t_7	delay, IOR* inactive to IOR* or IOW* active	2		cycles
t_8	delay, IOR* active to DATA low impedance	4	20	ns
t_9	delay, IOR* active to DATA valid	4	40	ns
t_{10}	hold time, IOR* inactive to DATA, CS*, RS[4:0] invalid	2		ns
t_{11}	delay, PCLK rising edge to READY* active	4	20	ns
t_{12}	delay, IOR* active to READY* active	1	1	cycles
t_{13}	pulse width, READY*	2	2	cycles
t_{14}	delay, PCLK rising edge to READY* inactive	4	20	ns
t_{15}	delay, IOR* inactive to DATA high impedance	2	20	ns

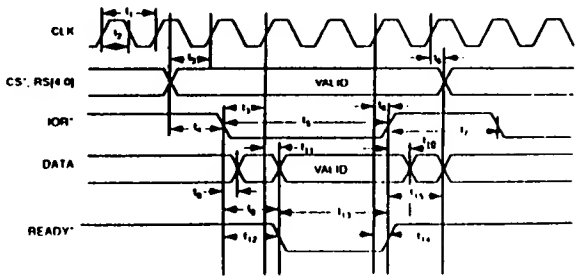


Figure 5-7. Read Timing (Local Hardware Interface)

CL-PX2070
Video Processor

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5.4.9 I/O DMA Timing (Local Hardware Interface)

Table 5-8. Local Hardware Interface Mode DMA Timing

Symbol	Parameter	MIN	MAX	Unit
t_1	period, PCLK			ns
t_2	pulse width, PCLK			ns
t_3	setup time, DMACK*, IOR*/IOW*, CS*, BLAST* active to PCLK rising edge			ns
t_4	delay, DMACK* active to CS* active			cycle
t_5	delay, CS* active to IOR*/IOW* active			cycle
t_6	delay, CS* active to IOR*/IOW* inactive			cycles
t_7	delay, IOR*/IOW* active to CHRDY* active			cycles
t_8	delay, PCLK rising edge to CHRDY* active			ns
t_9	delay, PCLK rising edge to read DATA valid			ns
t_{10}	hold time, PCLK rising edge to read DATA invalid, READY inactive			ns
t_{11}	delay, PCLK rising edge to IOR*/IOW*, CS*, BLAST*, DMACK* inactive			ns
t_{12}	setup time, write DATA valid to CHRDY* active			ns
t_{13}	hold time, write DATA valid to PCLK rising edge			ns
t_{14}	delay, PCLK rising edge to READY* inactive			ns
t_{15}	delay, IOR* inactive to DATA high impedance			ns

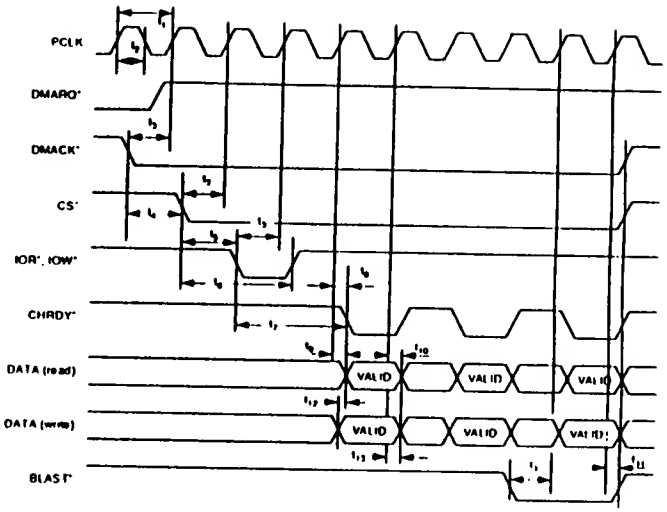

Figure 5-8. DMA Timing (Local Hardware Interface)

5.4.10 Input Video Timing

Table 5-9. Input Video Timing

Symbol	Parameter	MIN	MAX	Unit
t_{ps}	phase setup to clk	10	-	ns
t_{ph}	phase hold from clk	2	-	ns
t_{dout}	data, sync, blank valid after clk	5	15	ns
t_{IENV}	ien valid after clk	5	15	ns
t_{IENS}	ien setup time	10	-	ns
t_{IENH}	ien hold time	2	-	ns
t_{DIS}	data, syncs, blank setup time	10	-	ns
t_{DIH}	data, syncs, blank hold time	2	-	ns

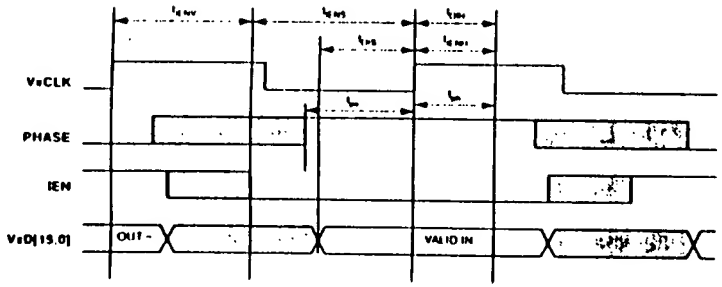

Figure 5-9. Input Video Timing

CL-PX2070
Video Processor

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5.4.11 Input Video Timing

Table 5-10. Input Video Timing

Symbol	Parameter	MIN	MAX	Unit
	minimum clock period	33	-	ns
	minimum clock high period	12	-	ns
t_{SRS}	stall request setup time	10	-	ns
t_{SRH}	stall request hold time	2	-	ns
t_{STV}	stall valid after clock	7	20	ns
t_{STIV}	stall invalid after clock	7	20	ns

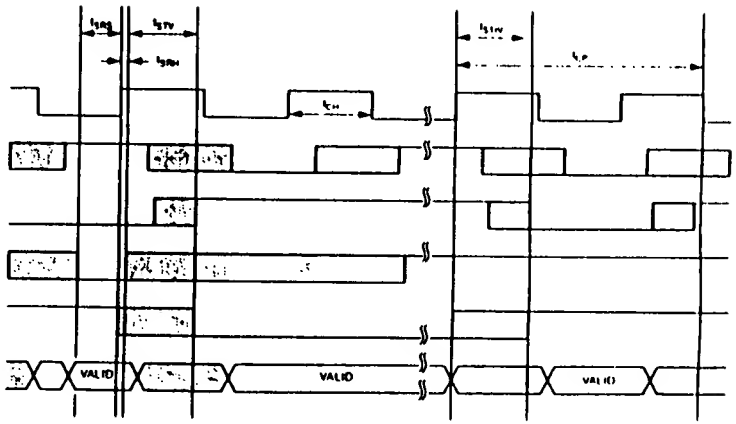

Figure 5-10. Input Video Timing

5. PACKAGE DIMENSIONS — 160-Lead PQFP

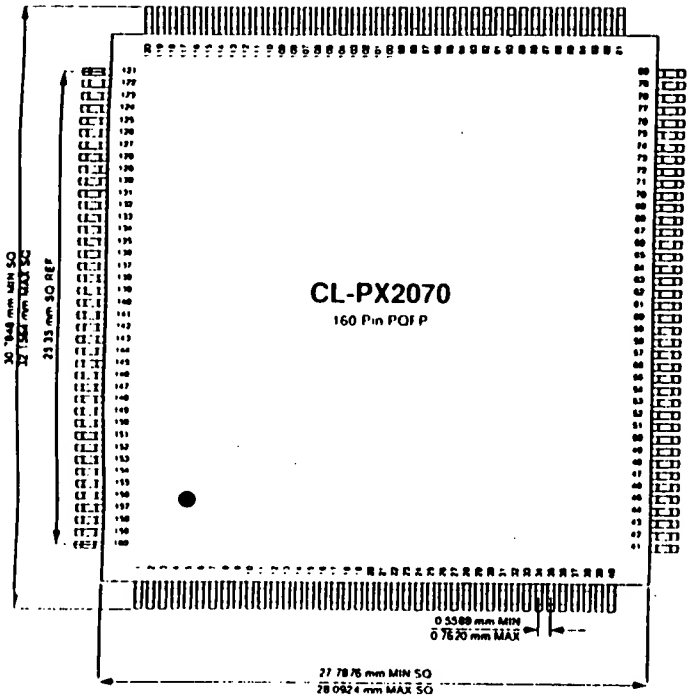

Figure 6-1. CL-PX2070 Package Information

CL-PX2070
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6. PACKAGE DIMENSIONS — 160-Lead PQFP (cont.)

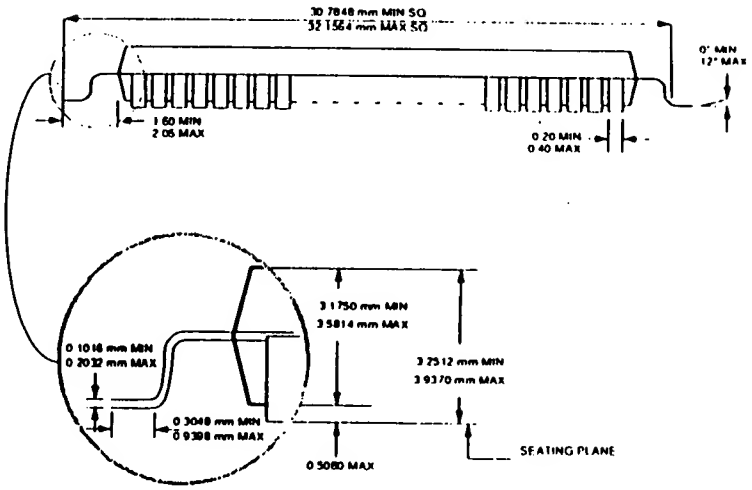
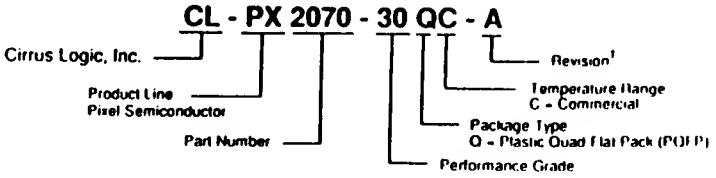


Figure 6-2. CL-PX2070 Package Information (Expanded View)

7. ORDERING INFORMATION

When ordering the CL-PX2070, use the following format:



[1] Contact Cirrus Logic for up-to-date information on revisions.

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NOTES

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NOTES

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FAX: 508/474-9149

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FAX: 908/603-7756

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FAX: 407/362-5235

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FAX: 81/3-5389-5540

SINGAPORE
TEL: 65/3532122
FAX: 65/3532166

TAIWAN
Taipei
TEL: 886/2-718-4533
FAX: 886/2-718-4526

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The Company

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